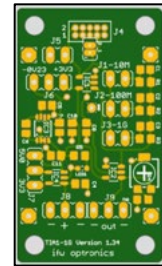


## Transimpedance Amplifier Board for Photodiodes JTIA1-1G

### Characteristics :

- ◆ for current/voltage-conversion and pre-amplification of photodetectors
- ◆ custom switchable transimpedance 10 M $\Omega$ , 100 M $\Omega$  and 1 G $\Omega$
- ◆ adjustable second stage amplification, range from 1x to 11x
- ◆ voltage output
- ◆ low dark offset
- ◆ single supply voltage
- ◆ pin headers for direct connection of all ifw-optronics SiC photodiodes
- ◆ RoHS und WEE conform



### Applications :

- ◆ prototyping; evaluation of SiC photodiodes
- ◆ general purpose photocurrent I/V converter
- ◆ use for single parts and small series production

### Absolute Maximum Ratings :

- |                       |                   |
|-----------------------|-------------------|
| ◆ supply voltage      | +28 V             |
| ◆ working temperature | - 25 °C ... 70 °C |
| ◆ storage temperature | - 25 °C ... 85 °C |

### General description :

The JTIA1 is a general purpose transimpedance amplifier board for photodiode measurements. The input-side can either be directly equipped with TO5 or TO18 photodiodes via multi-header or via pin-header for external connections. A transimpedance amplifier provides photocurrent-to-voltage conversion (between 0 - 5 V) on the output side.

### Gain Setting / Amplification:

The transimpedance gain can be set between three pre-configured values (10 / 100 / 1.000 M $\Omega$ ) via jumpers. This corresponds to a photocurrent amplification between 1V/nA and 0,1V/ $\mu$ A. A second-stage amplifier allows for the additional, variable amplification in the range between 1x and 11x via trim-pot. Custom values for feedback resistor and feedback capacitor can be manufactured or hand-soldered (package size 0805) by the customer.

### Power Supply:

The JTIA1 is internally regulated and supplied by a single-voltage supply between 6 V and 24 V and provides voltage output between 0 V and 5 V. For operation with 5 V supplies, the internal voltage regulator can be set to 3,3 V. In this case, the input voltage can be as low as 4,5 V, with the drawback of a decreased output voltage between 0 V and 3,3 V. A negative supply-voltage is generated internally for minimum offset-voltage and voltage-clamping.

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### Transimpedance Amplifier Board for Photodiodes JTIA1-1G

Functional Block Diagramm:

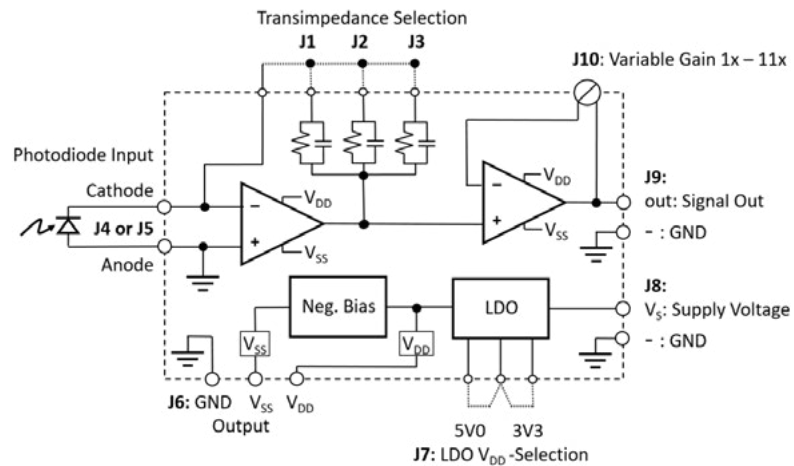


Figure 1: Internal 2-stage amplification circuit with voltage regulators

Electrical Specifications :

Parameter / Option	Test conditions	value	Unit
Power Supply Voltage $V_S$	Setting J7: 5V0 Setting J7: 3V3	+6 ... +24 +4,5 ... +24	V
Slew rate (J10: 1x / 10x)	10%/90% Setting J1: 1M (1 Gohm) <sup>1</sup> Setting J2: 10M (10 Mohm) <sup>1</sup> Setting J3: 100M (100 Mohm) <sup>1</sup>	6000 / 8000 30 / 50 500 / 600	$\mu$ s
Offset voltage max. (J10: 1x / 10x)	Input J4, J5: open	$\pm 1$ / $\pm 1$	mV
Dark offset voltage max. (J10: 1x / 10x)	$E = 0 \text{ lx}^{-1}$	$\pm 1$ / $\pm 2$	mV
Noise voltage (RMS) (J10: 1x / 10x)	Input J4, J5: open	0,7 / 6	mV
Saturation Output Voltage $V_{out}$	Setting J7: 5V0 Setting J7: 3V3	4,95 3,25	V
Short circuit current $I_{out}$	Setting J7: 5V0 Setting J7: 3V3	$\pm 90$ $\pm 50$	mA
Current consumption $I_S$	bright Setting J7: 5V0 ( $R_L = \infty / R_L = 2k\Omega$ ) <sup>1</sup> Setting J7: 3V3 ( $R_L = \infty / R_L = 2k\Omega$ ) <sup>1</sup>	7,6 / 10,0 5,5 / 6,0	mA
Max output current via output J6	3,3 V / 5,0 V 0,23 V	+ 5,0 -1,5	mA

common test conditions, if not specified otherwise:  $T_A = 25^\circ \text{C}$

<sup>1</sup>: with SiC photodiode JEA0,25 on input J4

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## Transimpedance Amplifier Board for Photodiodes JTIA1-1G

### Board Overview - Jumpers, Connectors:

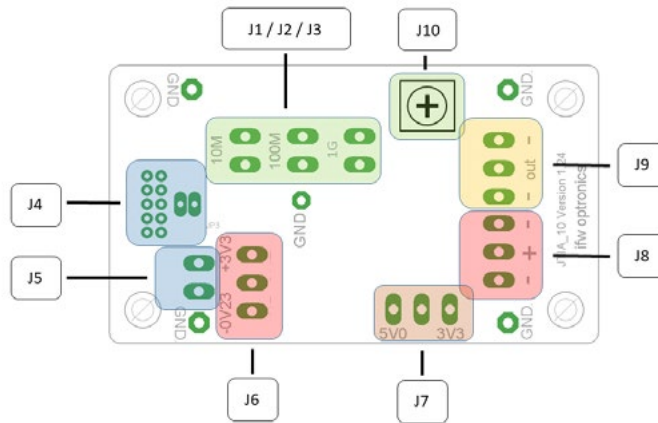


Figure 2: Schematic Overview of Jumpers, Connectors and Trimpots

### Jumper J1 / J2 / J3:

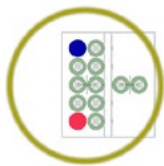
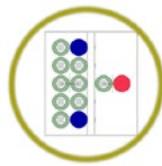
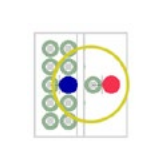
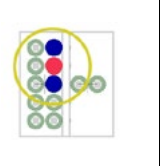
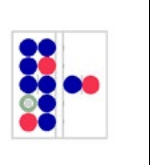
This set of jumpers sets the transimpedance gain of the first stage amplifier. Each jumper switches one feedback resistor and one feedback capacitor. The feedback capacitor is unpopulated by default, the parasitic capacitance is sufficient to damp the amplifier adequately. It is best practice to set only one jumper and leave the others unpopulated. To decrease amplifier- and signal-noise additional feedback-capacitance can be soldered next to the corresponding feedback-resistor.

Name	Board description	Value
J1	10M	(R1 / C1) 10 MOhm / 0 pF
J2	100M	(R2 / C2) 100 MOhm / 0 pF
J3	1G	(R3 / C3) 1.000 MOhm / 0 pF

### Input J4:

Multipurpose Photodiodes input. Photodiode connector with 5,08 mm and 2,54 mm grid dimension.

**Cathode to the input marked with red. Anode and case to ground marked with blue**

TO39, 2-pin	TO39, 3-pin isolated	TO18, 2-pin	TO18, 3-pin isolated	Overview
				
JEA1, JEAC1	JEA1I	JEA1S, JEA1SS	JEA1SZ	

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## Transimpedance Amplifier Board for Photodiodes JTIA1-1G

**Input J5:**

Photodiode input for external connections.

Pin-Name	Function
PD	Anode (+ Ground)
EXT	Cathode

**Output J6:**

Connector for internal regulated voltages:

Pin-Name	Function
-0V23	$V_{SS}$ : -0.232 V
Centerpin	GND
+3V3	$V_{DD}$ set by J7 (+5,0V, +3,3V)

**Jumper J7:**

Jumper for internal voltage regulator. For external supply voltages larger than 6V, choose setting "5V0" for maximum output voltage swing.

Connection	internal Voltage $V_{DD}$	Minimum Input Voltage
5V0 - Centerpin	5,0 V	6,0 V
3V3 - Centerpin	3,3 V	4,5 V

**Input J8:**

Power supply connector.

Pin	Function
-	GND
+	$V_S$
-	GND

**Output J9:**

Voltage output.

Pin	Function
-	GND
out	$V_{out}$
-	GND

**Trimpot J10:**

Trimpot sets second-stage gain between 1x and 11x. For lowest offset choose amplification 1x (turn fully counter-clockwise).

Function	Rotation
Increase gain	turn clockwise
Decrease gain	turn counter-clockwise

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### Transimpedance Amplifier Board for Photodiodes JTIA1-1G

**Mechanical Specifications :**

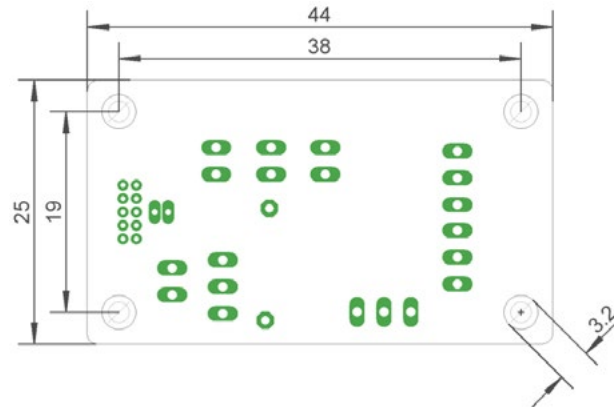


Figure 3: Mechanical Dimensions (mm)

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## Transimpedance Amplifier Board for Photodiodes JTIA1-1G

### Application notes:

- Use a regulated supply voltage  $V_s$  and prevent overvoltage situations on J7. The internal powersupply is only protected by a linear LDO regulator.
- Electromagnetic shielding has to be provided for the evaluation board and the optional connection from photodiode to the board.
- To reduce noise on the output additional feedback capacitance  $C_f$  can be soldered to J1. The pads C1, C2 and C3 correspond to the resistor values R1, R2 and R3. Increasing capacitance will reduce both noise and dynamic characteristics (slower rise-time) of the amplifier. A good starting point for  $C_f$  is 1pF.
- Avoid contamination of the PCB. Since high-ohmic feedback networks are employed, parasitic resistance between parts has to be kept low. If custom values of feedback resistors or feedback capacitors are soldered to J1, J2, J3, residual flux has to be removed.
- Pin-headers can be soldered in production or included separately to be soldered by customer
- Custom transimpedance values and feedback capacitance can be included during production. To be specified in the order.

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