Chip Documentation
SPAD2L192

Contents

1 Summary

SPAD2L192 is a SPAD-based line sensor for direct time-of-flight application. The sensor composes 2 x 192 pixels with 4 SPADs each for adjustable photon coincidence detection. Time measurement is performed by a partially in-pixel time-to-digital converter with a resolution of 312.5 ps and a full range of 1.28 µs.

2 Features

- Supply 3.3 V for electronics and 31 V for SPADs
- Two line 192 pixel
- Variable coincidence time, coincidence depth, and number of active SPADs
- Timing and counting mode

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3 Symbol and Pinout

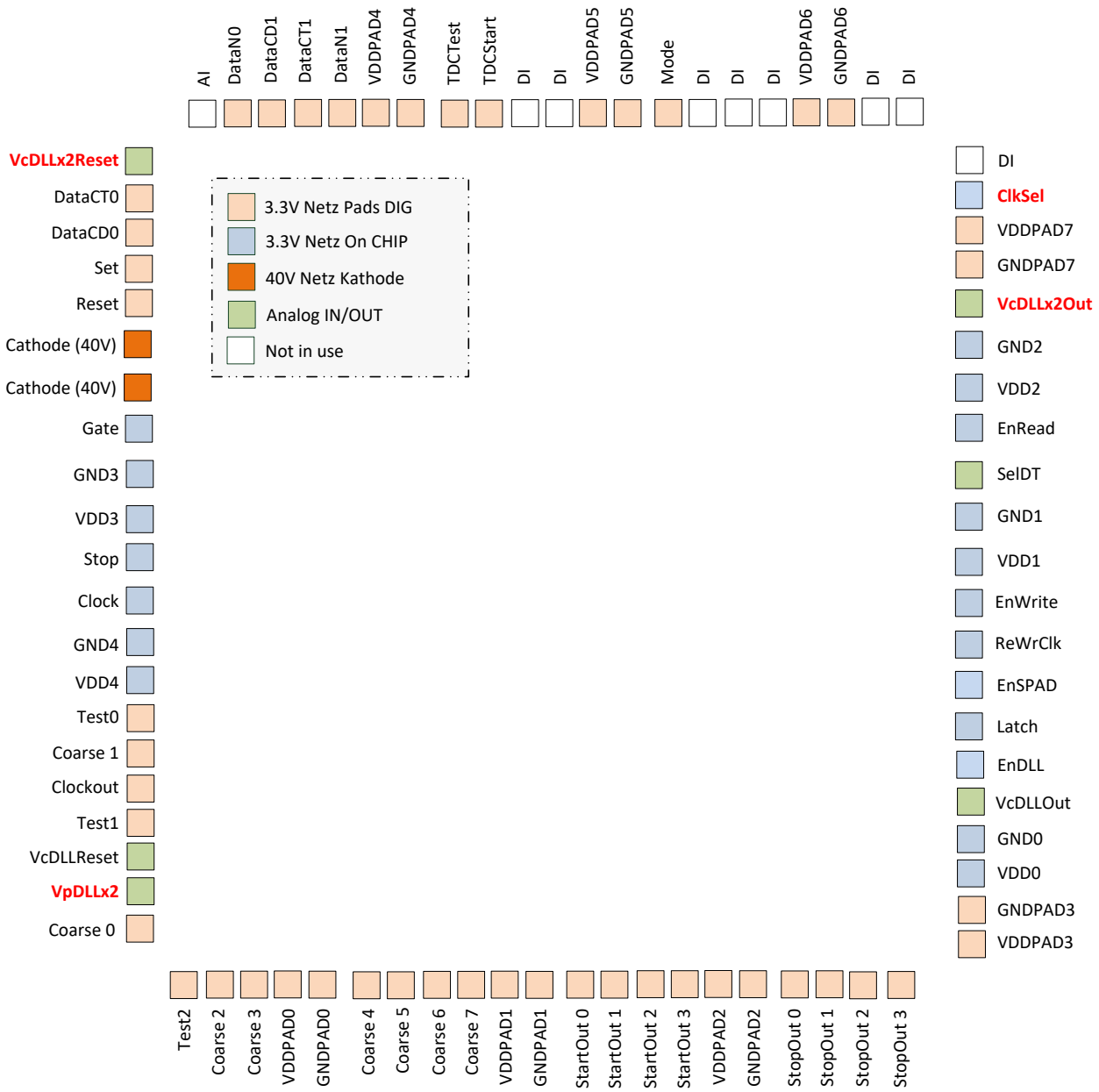

Figure 1: Floorplan SPAD2L192

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Table 1 Interface

Signal	Pin #	Type	Default	Description
Reset	5	DI	0	Resetting of the sensor
Set	4	DI	0	Enables clock signal for coarse time measurement
Gate	8	DI	0	Enables output of the SPAD frontend circuit, defines measuring window, enables SPAD
Stop	11	DI	0	Stops time measurement
EnSPAD	50	DI	0	Enables SPAD (OR connected with Gate)
Clock	12	DI	-	100 MHz input clock for the DLL
EnDLL	48	DI	1	Enables control signal for in-pixel DLLs, turn off for power saving
ClkSel	62	DI	0	Enable DLLx2 bypass
EnRead	56	DI	0	Enables clock signal for data readout
ReWrClk	51	DI	-	20 MHz clock signal for data read and write
EnWrite	52	DI	0	Enables clock signal for data write
Mode	71	DI	0	Switch between timing (0) and counting (1) mode
DataCT0/1	2/81	DI	0	Input data for coincidence time (CT) for the lower (0) and upper (1) pixel line
DataCD0/1	3/82	DI	0	Input data for coincidence depth (CD) for the lower (0) and upper (1) pixel line
DataN0/1	83/80	DI	0	Input data for number of active SPADs for the lower (0) and upper (1) pixel line
Latch	49	DI	0	Applies input data to pixel circuit
TDCTest	77	DI	0	Enables TDC test mode
TDCStart	76	DI	0	Starts time measurement in TDC test mode

Signal	Pin #	Type	Default	Description
VcDLLx2Reset	1	AI	2.0 V	Reset voltage of DLLx2 (clock doubling)
Cathode	6/7	AI	31 V	Cathode voltage of the SPADs
VcDLLReset	19	AI	1.0 V	Reset voltage of the DLL
VpDLLx2	20	AI	1.3 V	External control voltage of DLLx2
SelDT	55	AI	2.0 V	Controls the SPAD dead time

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Signal	Pin #	Type	Description
Coarse	21, 16, 23, 24, 27…30	DO	Output of the counter
StartOut	33…36	DO	Output of the start interpolator
StopOut	39…42	DO	Output of the stop interpolator
Test0/1/2	15/18/22	DO	Test outputs: DLL phase 2/3 and sampling

Signal	Pin #	Type	Description
VcDLLOut	47	AO	Control voltage of the DLL
VcDLLx2Out	59	AO	Control voltage DLLx2 output for testing

4 Timing

4.1 Startup

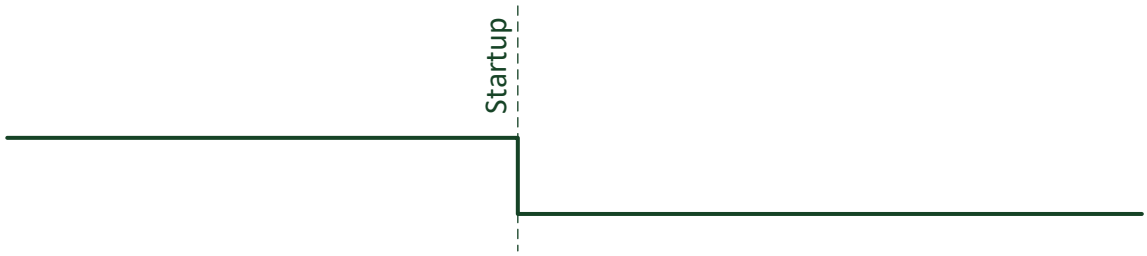

Figure 2: Timing sensor startup

After powering up the FPGA the **Reset** signal has to be set to high. Initiated by an external control signal **Reset** must switch to low signal. Now the sensor is ready for operation.

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4.2 Timing Mode

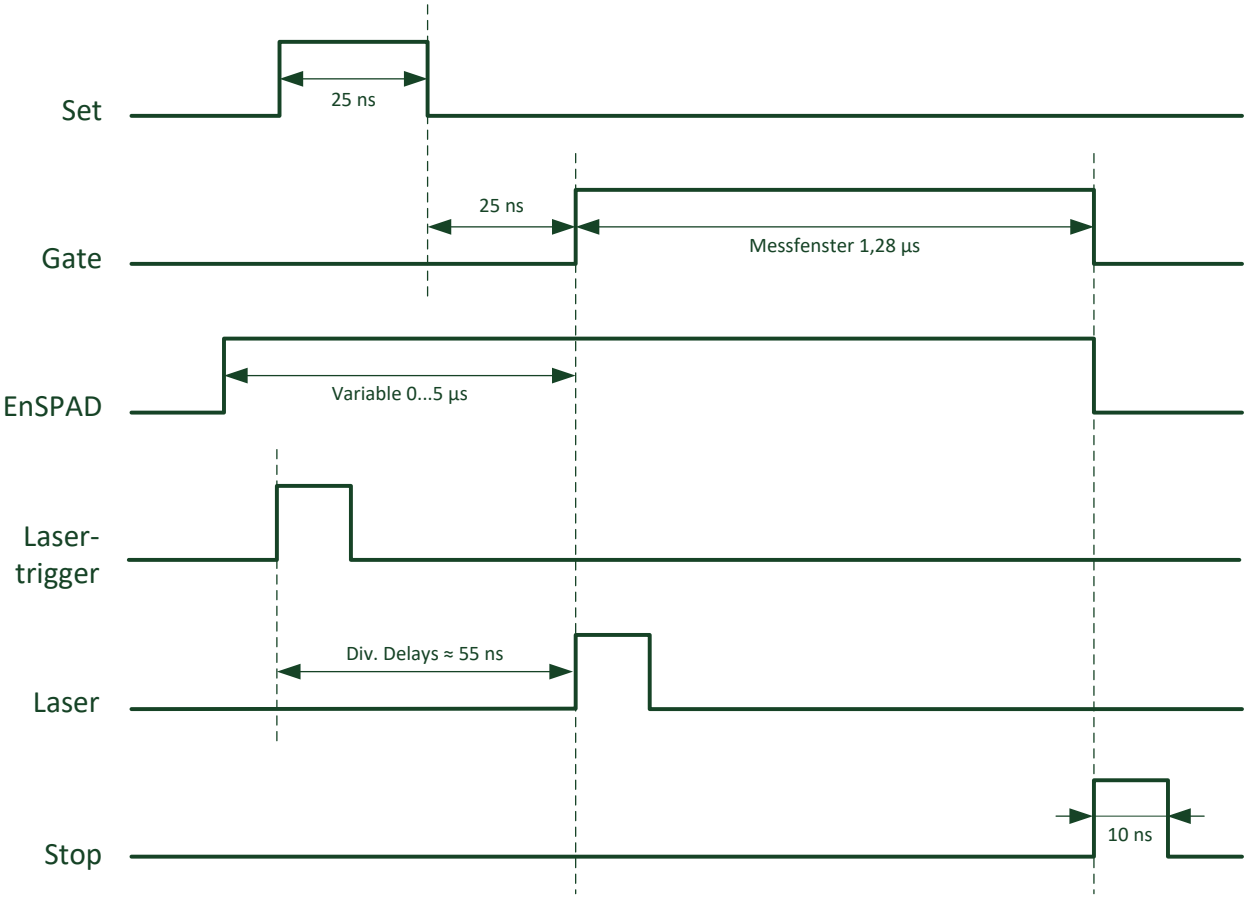

Figure 3: Timing sensor operation in timing mode

Before each time measurement a short 25 ns pulse at the **Set** signal is necessary to enable the 200 MHz clock for the coarse time measurement. After a short break of 25 ns the **Gate** signal is set to high to enable the output of the SPAD frontend circuit. Now SPAD generated pulses are able to start the time measurement. In standard scenario the laser pulse should be emitted with the beginning of the measurement window defined by **Gate**. To compensate for delays the laser has to be triggered some time before **Gate** is set high. To avoid the SPAD being reset during the measurement window, the SPADs can be enabled some time before the measurement window by setting **EnSPAD** to high. Since **EnSPAD** and **Gate** are connected via an OR gate for SPAD activation, EnSPAD has to remain in high state at least till **Gate** is set high. At the end of the measurement window the **Stop** signal has to be set high for at least 10 ns to stop the time measurement and transfer the time data into the in-pixel memory ready for readout.

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4.3 Counting Mode

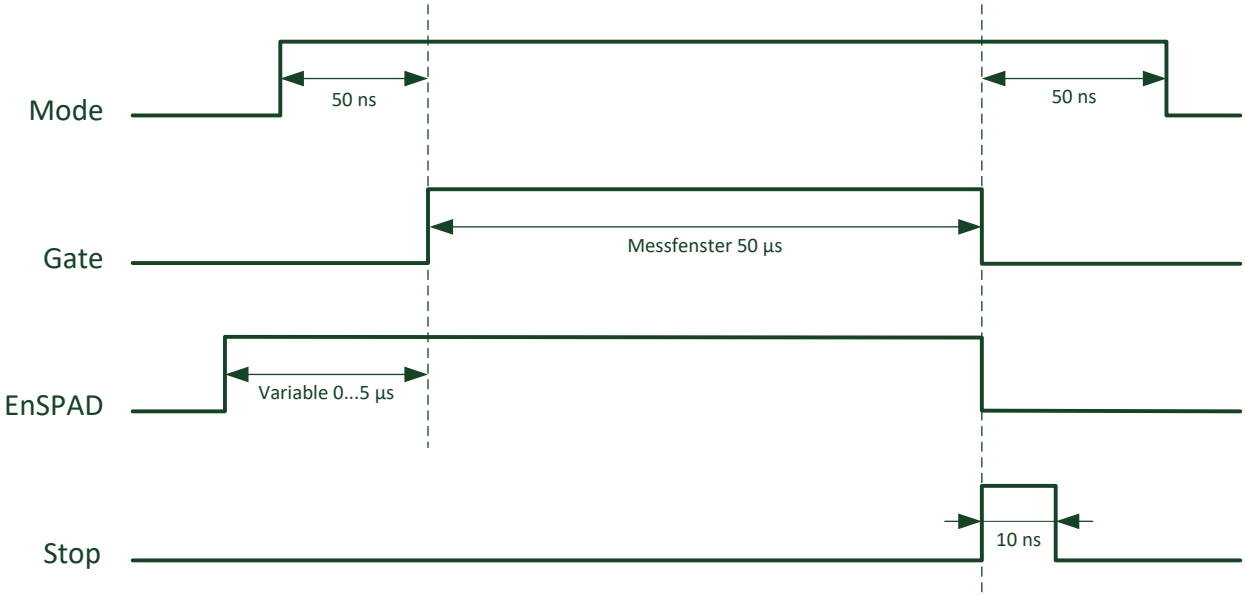

Figure 4: Timing sensor operation in counting mode

The count events the **Mode** has to be set to high. After a short break of 50 ns the **Gate** signal can be set high to enable the output of the SPAD frontend circuit. Now SPAD generated events are counted by the counter. After the measurement window **Stop** has to be set high for at least 10 ns to transfer the counter values to the in-pixel memory. As in timing mode the SPADs can also be enabled by setting **EnSPAD** high to avoid their reset within the measurement window.

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4.4 Readout

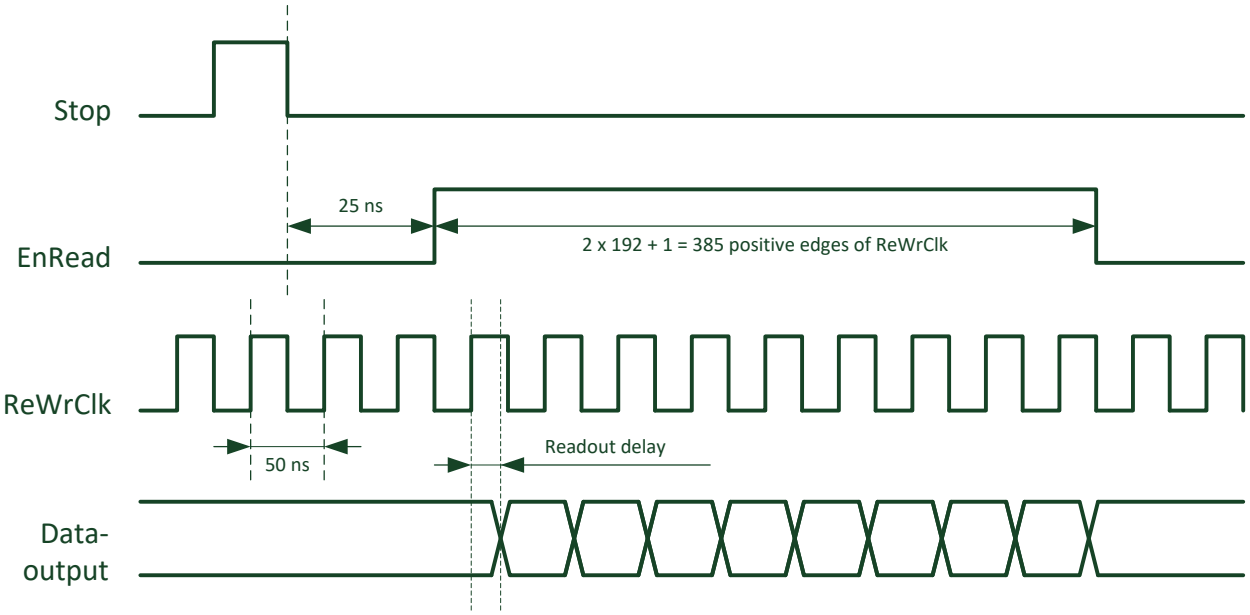

Figure 5: Timing sensor data readout

For data readout a short break of 25 ns between the **Stop** of the previous measurement has to be applied to transfer the data into the in-pixel memory. For readout the **EnRead** signal is set high at the falling edge of the **ReWrClk** and kept high for 385 clock periods. 384 clocks are for connecting the individual pixels to the readout bus while the last clock enables the internal pulldown buffers to avoid floating nets. Since the internal pixel change happens at the rising edge of the **ReWrClk**, the data should be captured at next rising edge to give enough time to process to the output pads.

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4.5 Write Data

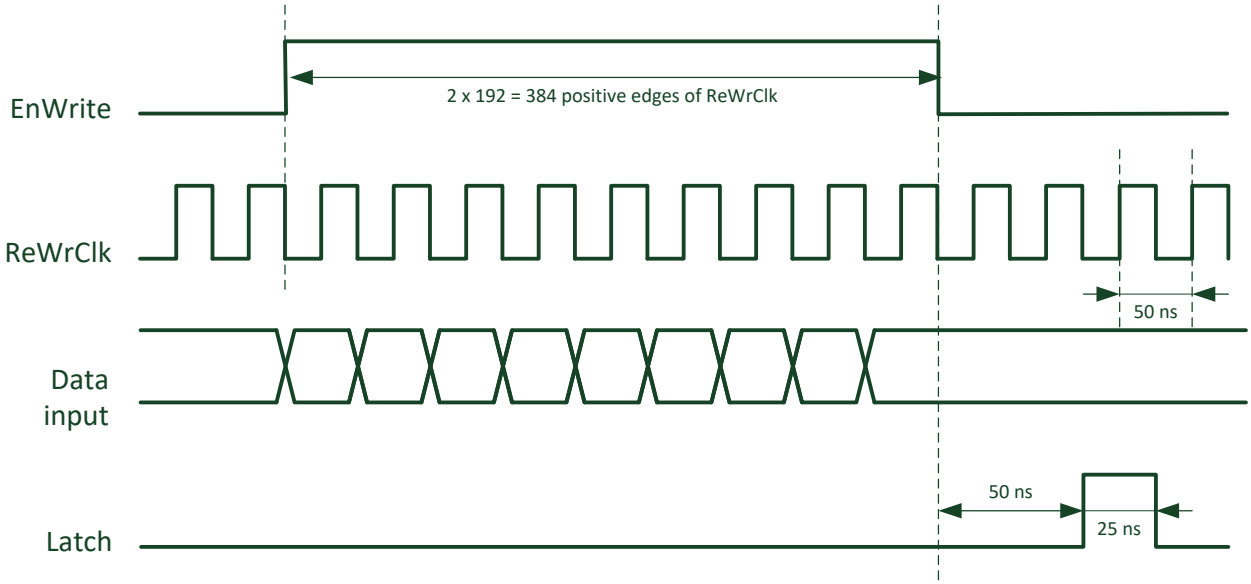

Figure 6: Timing sensor data writing

To write new data for the coincidence and enable SPAD registers, the **EnWrite** signal is set high at the falling edge of the **ReWrClk** and kept high for 384 clock periods. Since the data is internally captured at the rising edge of **ReWrClk**, the applied input data should be changed at the falling edge of the clock. After all data is written, at short pulse of 25 ns at **Latch** has to be applied to transfer the data from the shift register into the internal latches after a short break of 50 ns.

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4.6 Test Mode

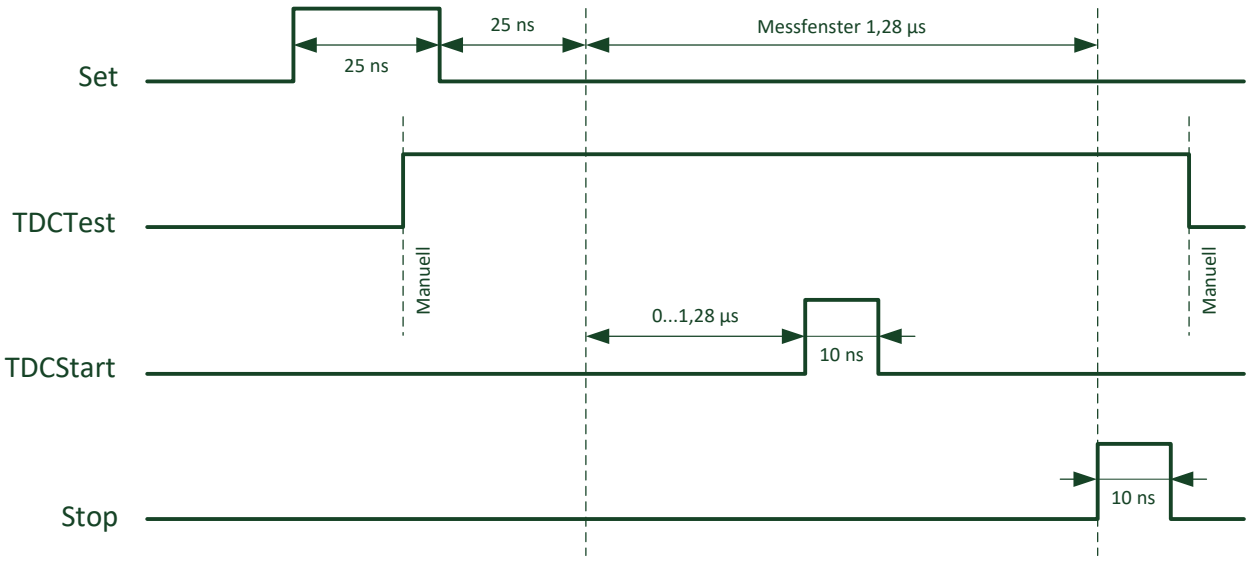

Figure 7: Timing sensor operation TDC test mode

In the TDC test mode the **TDCTest** has be set high. This can be done by the user. The enable the clock signal for coarse time measurement **Set** has to be set high for 25 ns before the measurements starts. The signal to start the time measurement **TDCStart** should be variable in time from 1,28 µs to 0 s before the **Stop** signal in steps of 312.5 ns or less. **TDCStart** and **Stop** signal must be high for at least 10 ns.

5 TDC Timing Calculation

The timing of the TDC is presented in Figure 8. The Start of the interpolator measures the time between start signal and the next positive edge of the clock. The next negative edge of the clock activates the counter and increments with the positives edges of the clock. The activation of the counter by the negative edge of the clock is taken by the synchronization circuit and therefore timing violations will be avoided. The same procedure will take place at the end of the measurement. The stop interpolator measures the time between the stop signal and the next positive edge of the clock. The stop of the counter will take place by the interruption of the clock at the next negative edge.

By means of the start interpolator N_{start}, the stop interpolator N_{stop} and the counter N_{coarse} the time T_{meas} can be calculated. It results in:

$$T_{meas} = \left(\frac{N_{start} - N_{stop}}{16} + N_{coarse} \right) T_{clk}$$

With the periodic duration of the clock T_{clk}. To enable a new measurement in the next cycle the clock will be activated before every measurement.

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The Data of N_{start}, N_{stop} and N_{coarse} is stored inverted in the sensor. The start and the stop interpolator is grey code coded. Thus, the data of N_{start}, N_{stop} and N_{coarse} has to be inverted first. Second N_{start} and N_{stop} has to be converted from grey code to binary.

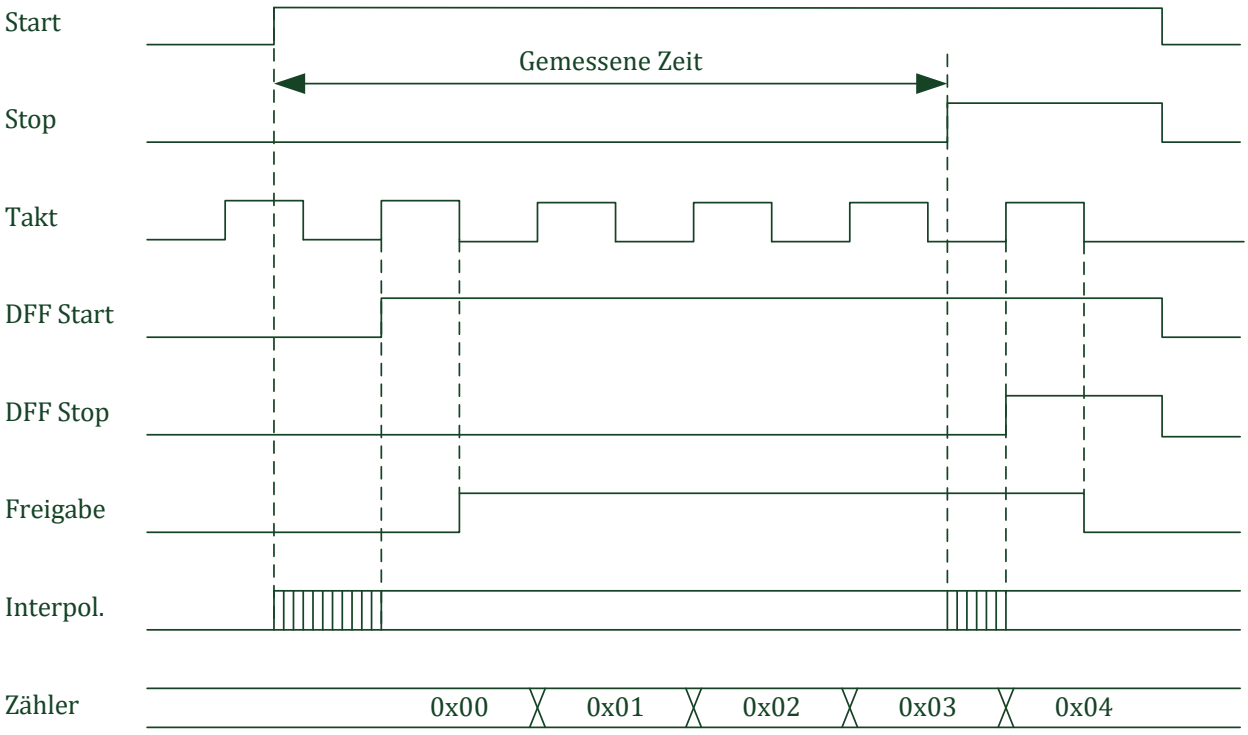

Figure 8: TDC timing diagram

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