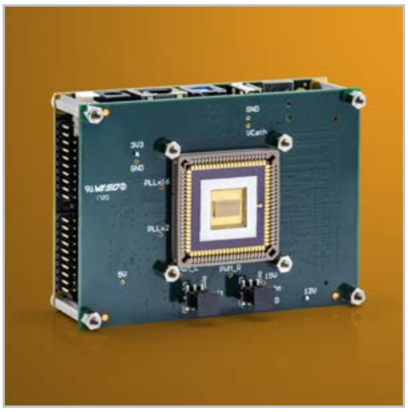
SPAD-LiDAR Evaluation Board



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www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
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Laser Components (UK) Ltd.
Tel: +44 1245 491 499
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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
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Tel: +1 603 821–7040
Fax: +1 603 821–7041
info@laser-components.com
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Tel: +33 1 39 59 52 25
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1. Description

The SPAD LiDAR Evaluation board provides the SPAD2L192 sensor with dedicated control system consisting of a sensor carrier PCB (Sensor-Board) and a SoC board (FPGA-Board). The custom-made carrier PCB includes reference and supply voltage and two delay lines to adjust the trigger delays (optional use). All control signals are generated by the SoC which is connected to the sensor PCB through FMC connector.

The whole system is supplied by SoC board's +12V DC jack and has a USB 3.0b socket for communication (only USB 2.0 is supported). All control functions and data are accessible via address over USB test and measurement protocol.

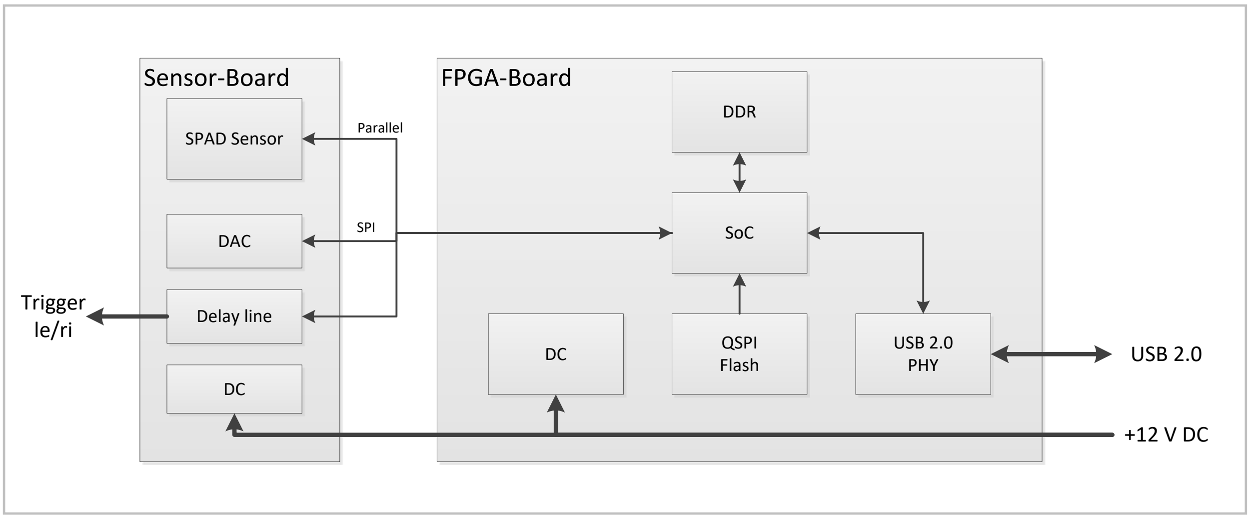

Figure 1: Block diagram of SPAD-LiDAR Evaluation Board

2. Components Required

- USB 2.0 A to B cable
- +12 V DC power supply (min. 1.5 A)

3. Set Up

Attention!

Please make sure your workspace is ESD-save before handling the devices!

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Laser Components S.A.S.
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The PLCC socket for the sensor and two trigger pin headers are located on the top of the PCB (Figure 2). The sensor is placed into the socket so that the sensor's position mark shows to the right side of the board (green arrow). Around the PLCC socket four M3 spacers (red circles) are affixed for e.g. mounting an optical lens in front of the sensor. The chip is arranged in a CQFJ84 housing.

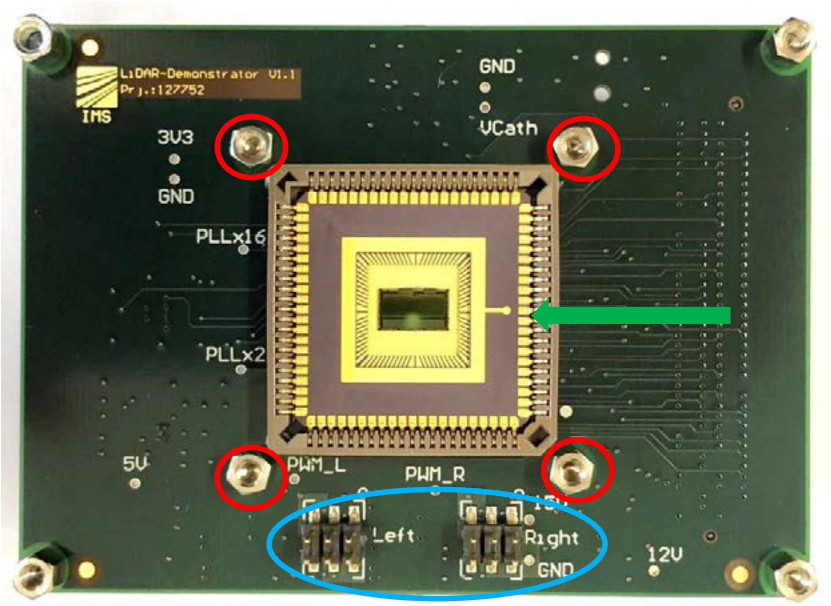

Figure 2: SPAD eval board top view
blue: triggers, red: optical fixture and green: positioning mark

Two trigger output pin headers (blue circle) offer a 15 V DC supply, GND, and a trigger pulse with 5 V amplitude. The width of trigger output pulse is configurable by software. The following table shows (Table 1) the allocation of each pin header.

Pin	Description
1	na.
2	GND
3	Trigger
4	GND
5	15 V DC (max. 500 mA)
6	nc.

Table 1: Allocation of trigger pin header

The SoC board is already connected to the sensor PCB and should not be dismantled.
The USB connection on the SoC board (blue circle, Figure 3) is used for communication with the PC.
The connector is USB 3.0 b standard but technically only USB 2.0 is supported, so that a USB 3.0 cable won't provide a velocity advantage. To operate the system, connect the SoC board to the PC with a USB 2.0 A to B cable.

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Tel: +33 1 39 59 52 25
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info@laser-components.com
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The DC jack (red circle) is suitable for 2.1 x 5.5 mm plugs with a supply voltage of 12 V and a minimum current of 1.5 A. All other connectors are non-functional, but could damage the SPAD-Line Eval Board if they are plugged.

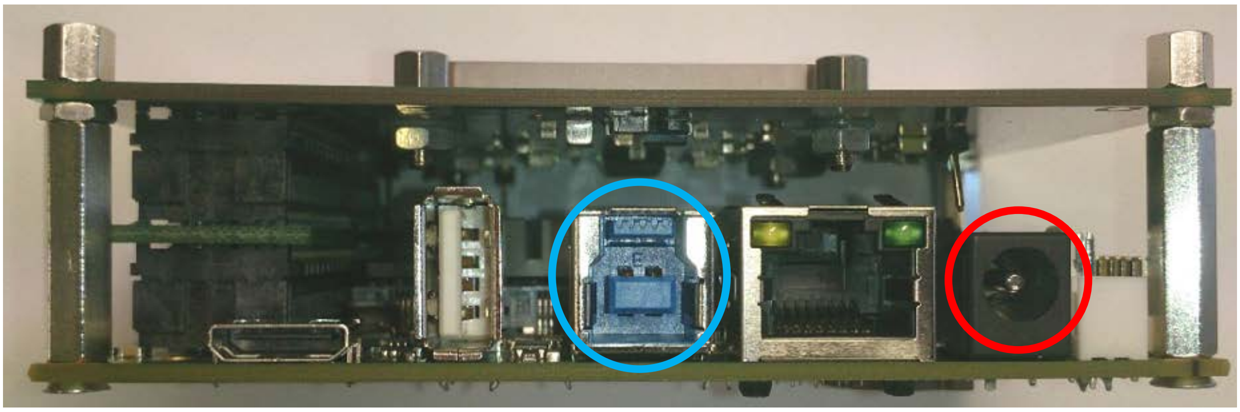

Figure 3: SPAD eval board side view (connectors)

4. Construction and Dimensions

The eval board can be mounted by four M3 spacers in the corners of the PCB and four M3 spacers around the PLCC socket. The focal plane of the chip is about 1.5mm shifted backwards in the PLCC socket. Here, production-related deviations can arise. In the next two figures you can see the dimensions of the connectors on the FPGA side and the arranged M3 spacers on the top of the PCB.

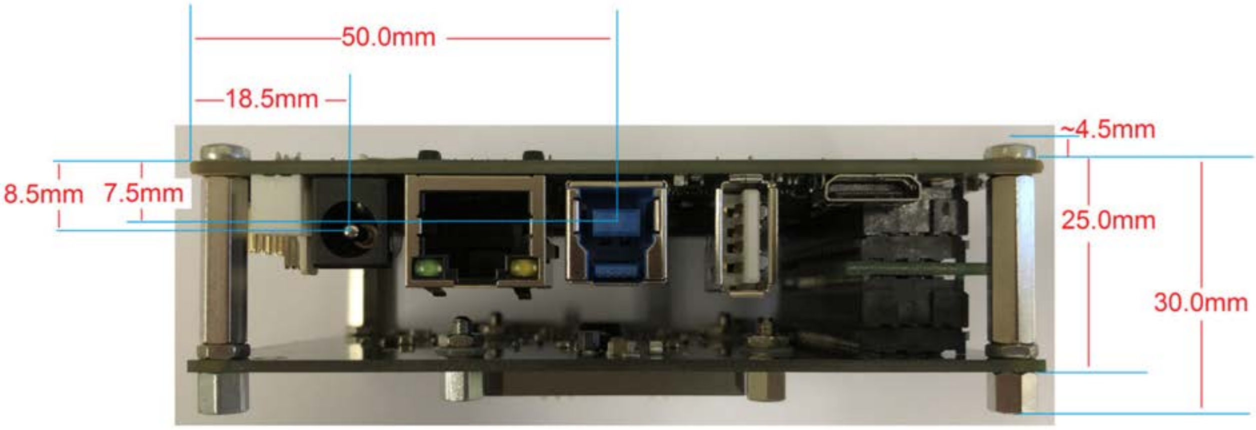

Figure 4: SPAD eval board side view (dimensions)

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Fax: +49 8142 2864–11
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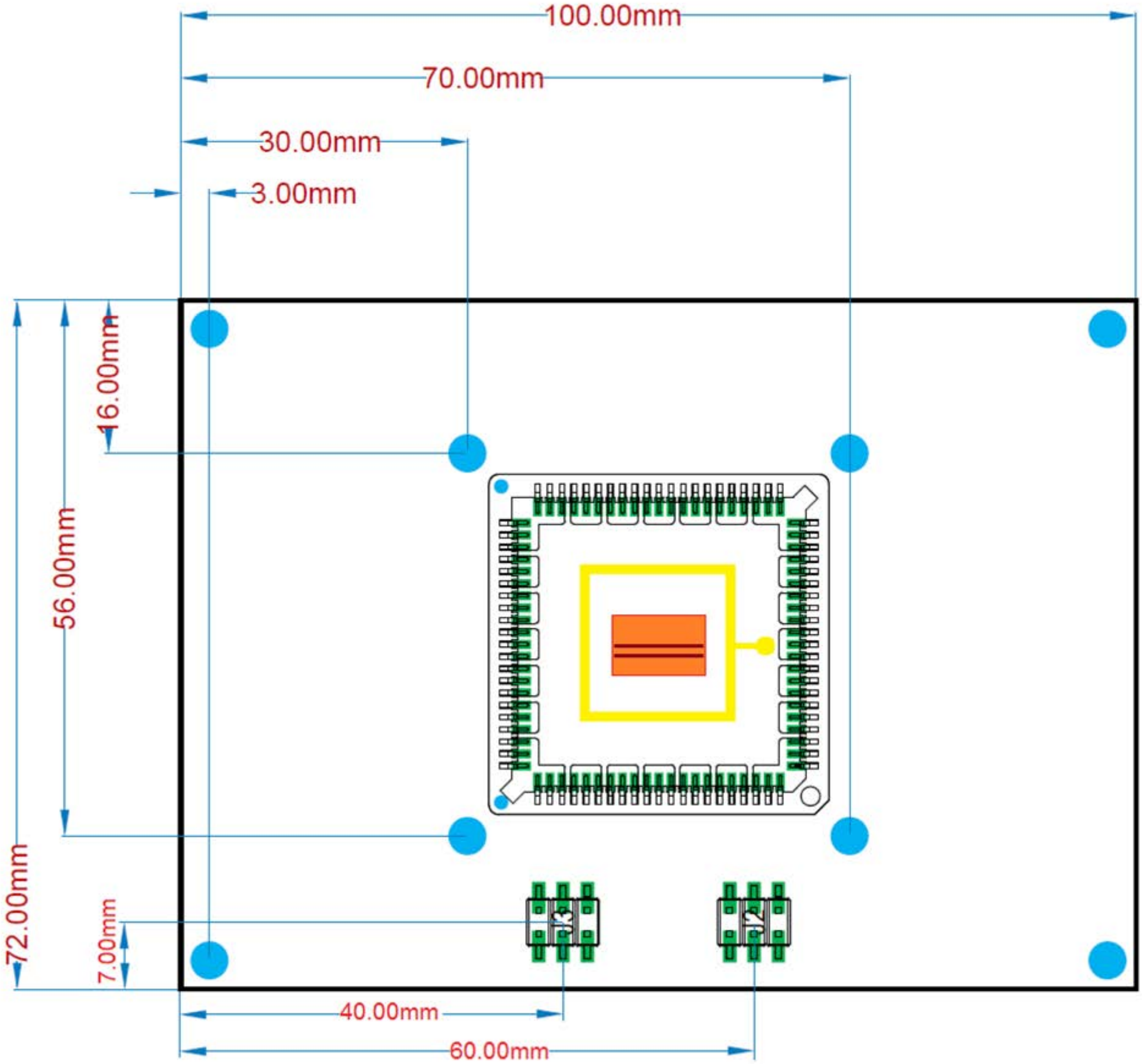

Figure 5: SPAD eval board top view (dimensions)

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Laser Components S.A.S.
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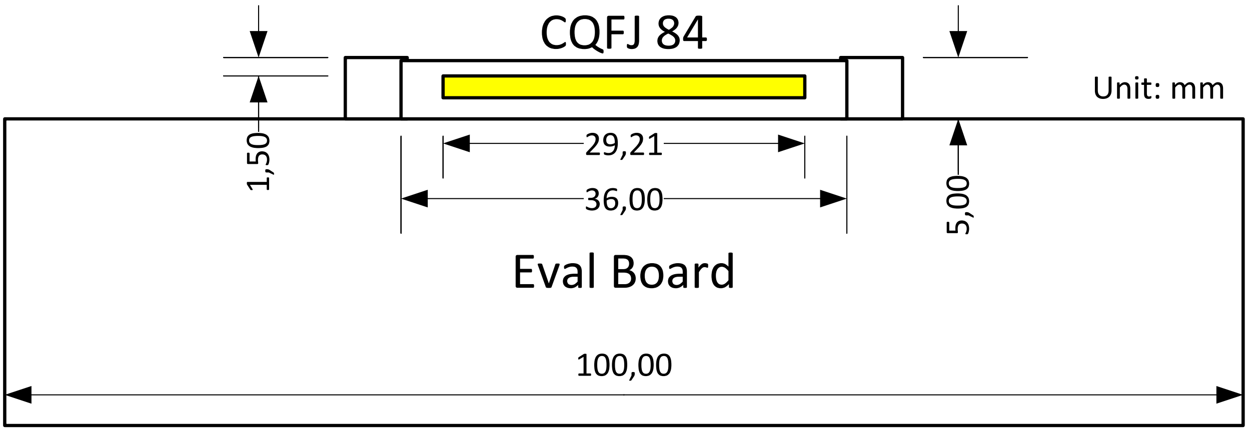

Figure 6: SPAD eval board side view with CQFJ 84 package (dimensions)

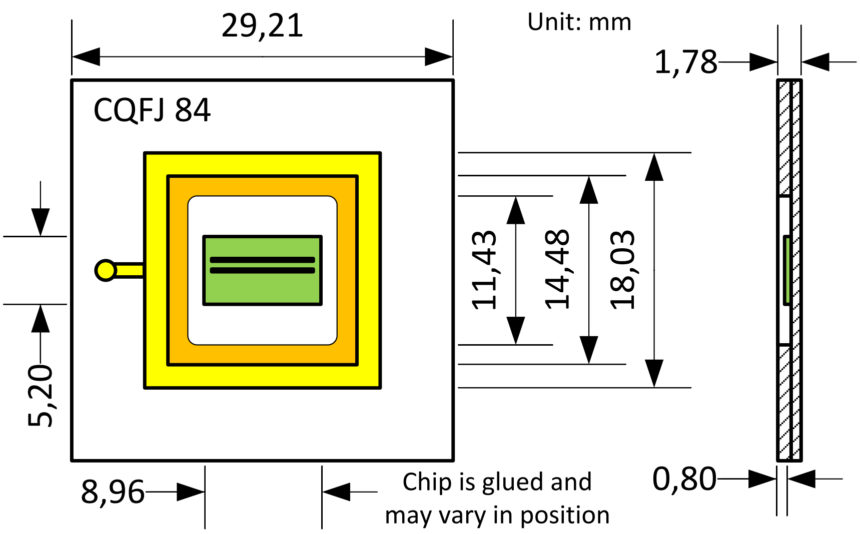

Figure 7: CQFJ 84 package with chip in the middle (dimensions)

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Laser Components S.A.S.
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Fax: +33 1 39 59 53 50
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Tel: +46 31 703 71 73
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Fax: +1 603 821–7041
info@laser-components.com
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5. Software Alternatives

The SPAD LiDAR evaluation board can be used either with the provided software for communication and visualization (LabView executable file) or with an own specific control software to directly access the FPGA firmware.
The LabVIEW executable provides the full communication and visualizing without any need to generate an own program.
Optional the communication can be programmed with an own specific software which allows then to integrate own analysis and data processing for specialized applications.
In section 6 the option for the LabVIEW executable and in section 7 the option for the self-programming code is described.

5.1 Driver

A Driver for "USB Test and Measurement Devices" from IVI Foundations is needed. It is included in National Instruments and also available from Agilent for instruments communication and the" Keysight Connection Expert".

6. LabVIEW Executable

In the following section the installation of the LabVIEW runtimes, the use of the executable and the software handling will be described.

6.1 Software Installation

The software to control the SPAD LiDAR Evaluation board is written in LabVIEW. To run the control program several LabVIEW-Runtimes have to be installed. The actual program based on the LabVIEW 2017 version.
A 32bit version is available.

6.1.1 LabVIEW-Runtime

The following Runtimes hast to be installed:
1. NI LabVIEW Runt-Time Engine
2. NI-VISA Runtime

For the runtime no payed license is needed.

The installation files of the runtime can be found at the National Instruments website http://www.ni.com
A free account has to be created to download the setup files from NI. Follow the installation instructions during the installation of the runtimes.

First install the main LabVIEW Run-Time Engine 2017:

32bit http://www.ni.com/download/labview-run-time-engine-2017/6819/en/

Second install the NI-Visa 17.0 Run Time Engine:

http://www.ni.com/download/ni-visa-run-time-engine/6647/en/

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www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
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Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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Fax: +1 603 821-7041
info@laser-components.com
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6.1.2 Eval board program

The eval board program called "SPAD-Line Eval Board" is an executable file and do not need to be installed. It has to be copied to any point of the computer. From there the .exe file in the folder can be executed to run the software.

6.2 Set up

Plug in the eval board with the USB A to B cable to the computer and connect the power supply. Make sure that the power supply is 12V.
After this the device "SPAD-Line Eval Board" should appear in **Control Panel > Hardware and Sound > Devices and Printers** (Figure 8). With the first connection, the automatic driver installation may take a little time.

Figure 8: Devices and Printers

If the eval board icon appears in Devices and Printers, it is ready to use.

6.3 Software documentation

The program can be used to display the photon detection rate of every pixel. Therefore a real time plot and everal history plots are available. In addition export functions allow the external analysis of data. The settings give extensive options to adjust the count of measurements, the accumulation time or the coincidence level. In addition trigger settings are available to trigger two external trigger signals.

6.3.1 Main window

6.3.1.1 Counting Mode

In Figure 9 a screenshot of the main window in counting mode is shown. It will be visible directly after start of the program. The main window gives in three different plots an overview about the counted photon events in every pixel of both SPAD2L192 lines.

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
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info@lasercomponents.com
www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
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Tel: +44 1245 491 499
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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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Figure 9: main window – counting mode[1]

The measurement can be started and stopped with the "run?" bush button. The "Stop" control (shown here in Figure 3) will stop the whole communication to the eval board and closes the program. LabVIEW has also a functionality to use a red dot in the menu bar to kill the program. This functionality should only be used if the "stop" button does not work.

The "frames/s" indicator shows the reached repetition rate of the measurements depending also on the computer engine. In addition, a sequential number of the displayed measurement is in "#measurement" shown. With the "save rate" and "save history" buttons it is possible to save the measurement data (see section 6.3.3). The "open settings" button will open an extra window to make different settings (see section 6.3.2).

The upper plot displays the real time rates of every pixel (x-scale). The y-scale is a logarithmic plot of the photon detection rate and will be automatically scaled. The red and the white plot each represent one SPAD line of the sensor SPAD2L192.

The other three plots in the main window are history plots. In the graph on the left single pixels with "row" and "pixel" can be addressed to record the photon detection rate in a history plot over several measurements. With the control "x-scale" the last x measurements can be displayed.

The plots on the right record the photon detection rate from each line separately. It is a color plot where the x-scale is the past time in history measurement data, the y-scale represents the pixel number of the SPAD line and the photon detection rate as "z-scale" is color coded and automatically scaled. The color from black over blue to white means low rates in black to high rates in white. With the "clear history" button the recorded history data can be reset and the three history plots will be cleared.

[1] An additional optic is needed to see an image in the color plot

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info@lasercomponents.com
www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
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info@lasercomponents.co.uk
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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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Laser Components USA, Inc.
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6.3.1.2 Timing Mode

In Figure 10 a screenshot of the main window in timing mode is shown. The timing and counting mode window can be changed via the tabulator "Counting Mode / Timing Mode". The upper plot displays the timing data histogram of one selected pixel. The bin size in the plot corresponds to 312.5 ps. The displayed range can be changed by the "range" control. The lower plot shows a color plot of all pixels timing data. The x-axis shows the pixel number where pixel 0-191 are the first and 192-383 are the second row. The y-axis shows the bin value and the z-axis corresponds as color to the counts in the bin. The color form back over blue to white represents to the counts.

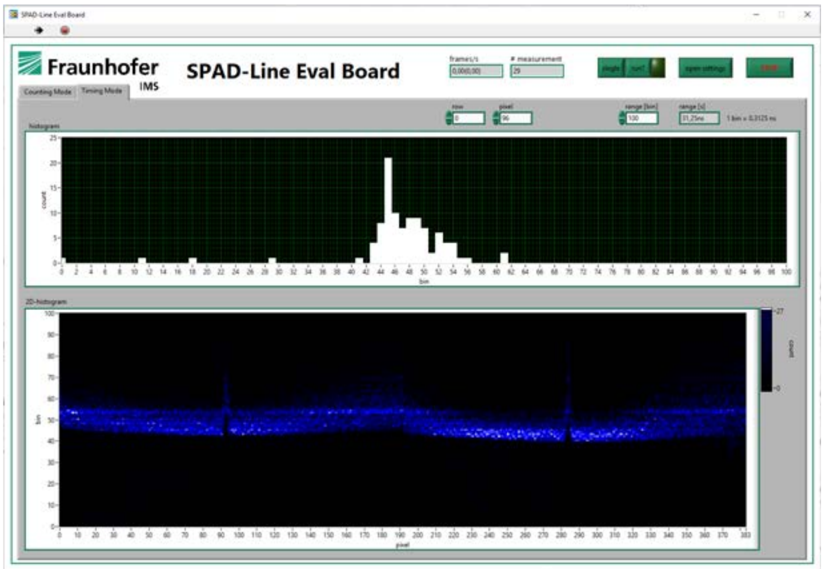

Figure 10: main window – timing mode[2]

6.3.2 Settings

The settings window (Figure 11) is grouped into four boxes. In "measurement setting" the duty cycle can be set in 6.25 ns steps. This is inverse proportionality to the duty frequency. Also, the measurement count for accumulation can be chosen. The "duty (approx.)" indicator shows the resulting duty cycle with all limitation settings.

[2] An additional optic is needed to see an image in the color plot

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Laser Components S.A.S.
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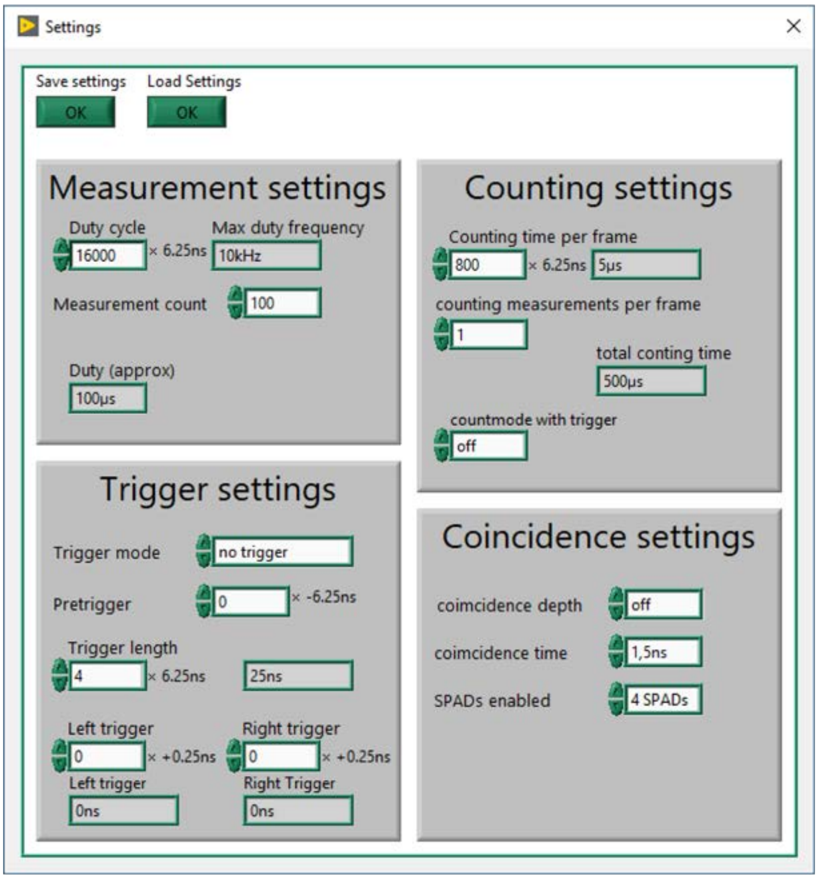

Figure11: settings window

Among "counting settings" the counting time in one measurement frame can be set in which the photon events are counted. It is also specified in 6.25 ns steps. The integrated counter in the pixel has only 8 bit and so on the maximum number of counts in one period is 255. If 255 is counted and there will be a further event, the counter will reset to 0 without an overflow flag. A counting time of 800 (5 µs) is a good choice to not overflow also at high rates. The total counting time results by the counting time multiplied with the measurement count per frame. By activating the setting "countmode with trigger" the timing mode will be disabled and at the beginning of a counting measurement the Trigger Channels are triggered (see Figure 23).

The "trigger settings" are important when combining the evaluation board with an external laser source. Two different sources (right and left) can be operated. In the trigger mode the right, the left channel, both channels or no channel can be chosen. With the "pretrigger" control the trigger signal can be changed in negative -6.25 ns steps for both channels simultaneously. In addition to the "pretrigger" each channel can be time adjusted separately in „left trigger" and "right trigger" in positive 0.25 ns steps. The trigger length of the two channels can be controlled by "Trigger length" control in 6.25 ns steps.

In the bottom left box, the "coincidence settings" allow to set the coincidence circuit of all pixels. The coincidence function is based on Fraunhofer IMS IP which firstly can be used with SPAD2L192 and this evaluation board. Especially with high background light by the sun during outside measurements the coincidence levels should be adjusted for an optimum sunlight suppression.
Each pixel of the detector consists of four SPADs for the coincidence detection. If a certain number of photos, called coincidence depth, detected by the different SPADs within the pixel and a certain time, called coincidence time, a coincidence event is detected (Figure 12).

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
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Tel: +46 31 703 71 73
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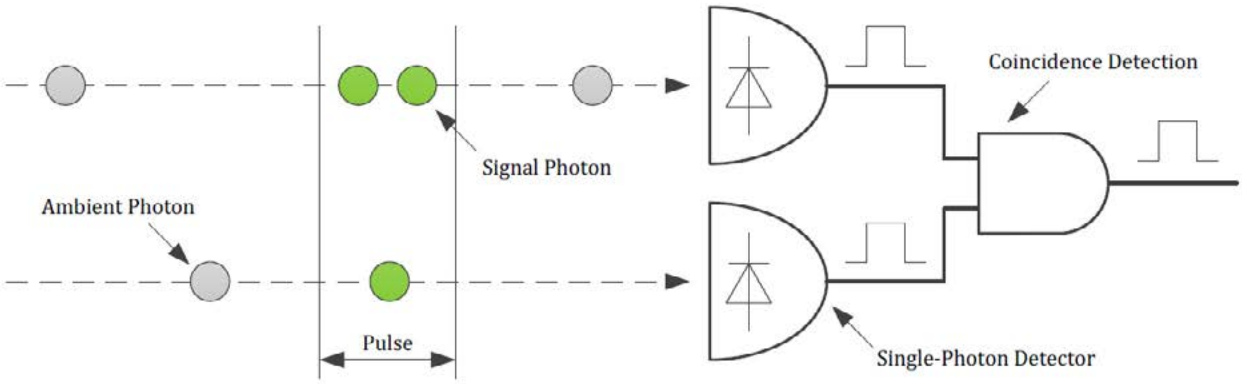

Figure 12:
Simple illustration for the detection of coincidence events. If the output pulses of the detectors with a width corresponding to the coincidence time overlap, a coincidence event is detected.

At every start of the program the default settings are loaded. All changes in the settings can be saved by using the "save settings" button. With the "load settings" button these configurations can be easily loaded and used.

6.3.3 Export data

It is possible to save the data of the plots in a .csv file. The "save rate" button in the main window will save the actual photon detection rate of both lines. A window like in Figure 14 will appear and you can save the .csv file.

In format of the file will be:

Line 0 pixel 0; line 0 pixel 1; …; line 0 pixel 191

Line 1 pixel 0; line 1 pixel 1; …; line 1 pixel 191

To save the recorded history data press the "save history" button. It can save up to 100,000 history measurements which is not limited to the displayed values in the plots. The window in Figure 13 will appear and the data source can be selected: the history data of the selected single pixel, the history data of the whole line 0 (upper) or the whole line 1 (bottom). A multi selection is possible. For each selection a separate file save dialog will appear (Figure 14).

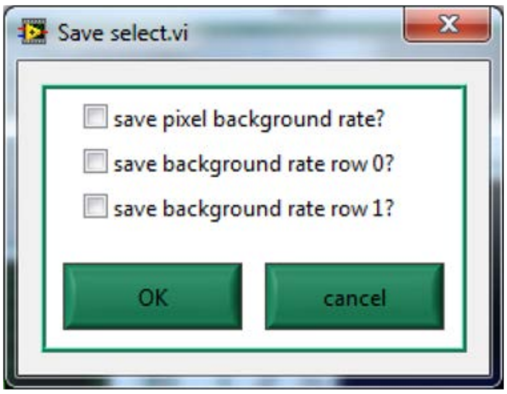

Figure 13: save select

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Fax: +49 8142 2864–11
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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
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Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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Laser Components USA, Inc.
Tel: +1 603 821–7040
Fax: +1 603 821–7041
info@laser-components.com
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The format of the .csv for the single pixel is:

Measurement 0; measurement 1; …; measurement n

The format of the whole row selection is:

Measurement 0 pixel 0; measurement 0 pixel 1; …; measurement 0 pixel 191
Measurement 1 pixel 0; measurement 1 pixel 1; …; measurement 1 pixel 191
…
Measurement n pixel 0; measurement n pixel 1; …; measurement n pixel 191

Measurement 0 is the oldest measurement and measurement n is the newest one.

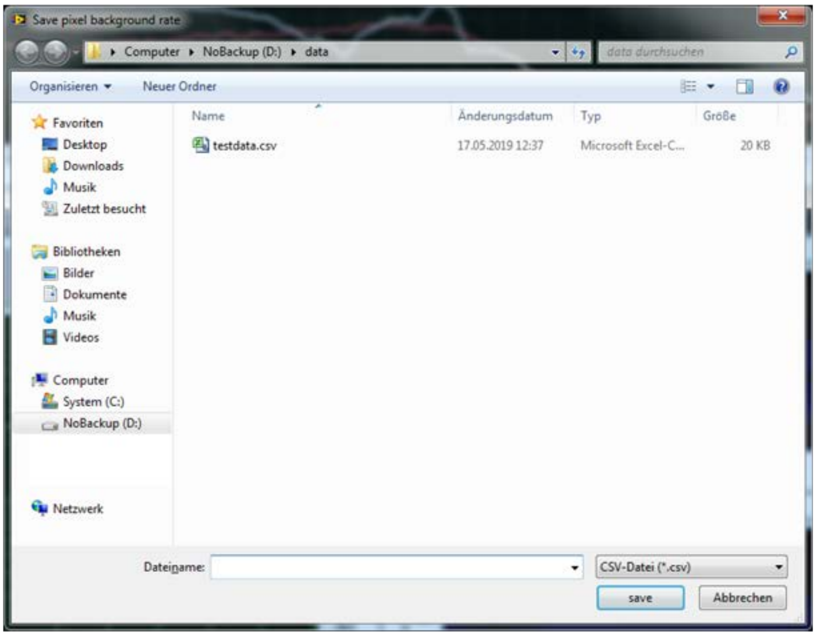

Figure 14: file save

6.4 Error handling

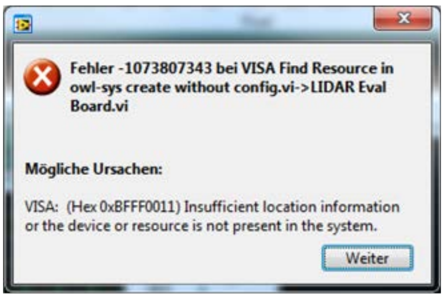

Figure 15: error no LiDAR camera

The error in Figure 15 appears if the connection of the SPAD-Line Eval Board is not correct. Close the software; unplug the USB cable and the power supply. Then connect the USB cable and power supply again, check whether "LiDAR sensor control board" appear in Control Panel > Hardware and Sound > Devices and Printers (Figure 8) and start the software again.

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Fax: +33 1 39 59 53 50
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info@lasercomponents.co.uk
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7. Programming Specific Software

In the following sections the communication to the FPGA, the access to the firmware and the sensor timing will be explained in detail. For consideration in chapter 8 the known bugs are listed.

7.1 Communication

The SoC functions can be accessed over USB test and measurement class protocol via address and, where required, data input.

For easy integration into software the following tools are recommended:

- National Instruments Measurement & Automation Explorer (MAX) or
- MatLab Test & Measurement Tool available in different Toolboxes.

If one of these tools is installed on your PC the SPAD-LiDAR Evaluation Board should be automatically recognized as USB test and measurement device on USB port at first startup. In the device and printer window of the PC "SPAD LiDAR Eval Board" should be displayed.

The control commands of the Eval Board exist of an address and – if necessary – followed by data. All addresses are listed in section 7.3 were an 8 bit address is separated in a base and offset address. Base addresses are 4 bit long and classify the offset addresses (4 bits). A multiplication (logical OR) of base address and offset address will give the complete address to be send to the Eval Board.

If data is required in addition to the address data, it will follow in a multiple of bytes, even if the relevant data bits are less than a byte.

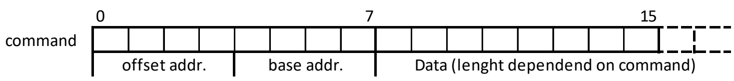

Figure 16: Bitmap of command

Frame data acquired during the measurement is buffered in DDR memory and has to be downloaded regularly while measurement is running. This is done by a request of the USB host (PC). Each data packet has 768 and 384 bytes, respectively, additional to a 4 byte header including frame count and acquisition mode information. If no data is available a zero length packet will be responded.

A packet transfer starts with the header (Figure 17). It shows in the first 16 bits the frame counter of the measurement, in bit 16-18 the counter of backlight (BL) measurement and in bit 29-32 the acquisition mode.

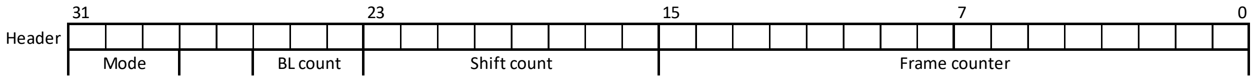

Figure 17: Bitmap data packet header

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
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info@lasercomponents.co.uk
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Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
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Fax: +1 603 821–7041
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The following data length differs by acquisition mode and is indicated by three bits. The following Table 2 shows the mode and amount of data bytes.

Bit mask	Mode	Data bytes
0b001	Test	0
0b010	Backlight	384
0b100	Normal	768

Table 2: Acquisition mode bit mask

In backlight acquisition mode BL count displays the actual backlight measurement.

In normal acquisition mode pixel data is transferred with rising pixel number every 2nd byte. Each pixel data is separated into 4 bit Stop and 4 bit Start followed by 8 bit coarse values (Figure 18).

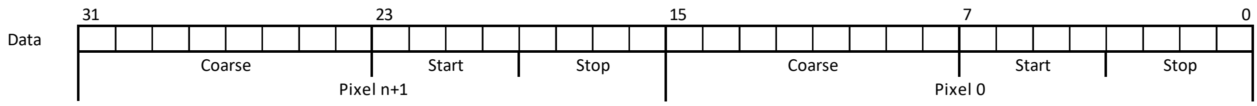

Figure 18: Bitmap data packet normal mode

In backlight acquisition mode pixel data is transferred with rising pixel number every byte and consists only of coarse value (Figure 19).

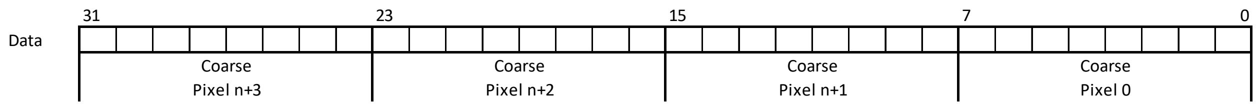

Figure 19: Bitmap data packet backlight

In test mode only the header is transferred with the data in the least 15 bits (Figure 20).

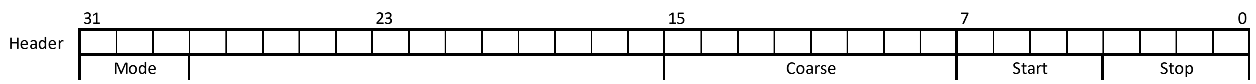

Figure 20: Bitmap data packet test mode

A description of coarse, start and stop values can be found in section 5.2.3.

The readout order starts with pixel 1 of the lower row up to pixel 192 and continues with pixel 193 of the upper row up to pixel 384 in one sequence (see Figure 21).

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Fax: +46 31 703 71 01
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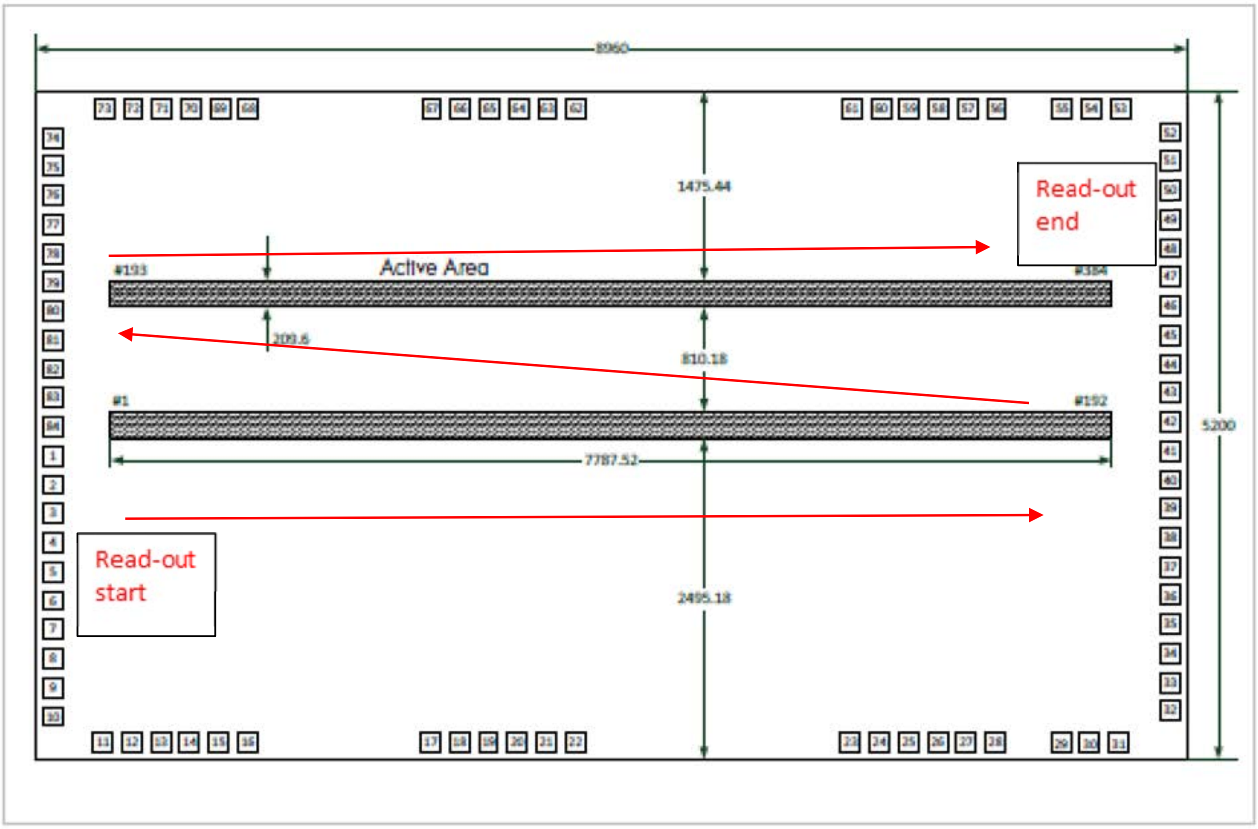

Die Drawing (all metrics are given in µm)

Figure 21: Chip drawing with readout order

7.2 Firmware

After system startup (power on) the supply and reference voltages are activated and the sensor is hold in reset state. After this the user has to initialize the system by setting the MEAS_RESET address. This initials the system to:

- 400 measurements
- 10 kHz repetition rate
- 25 ns trigger pulse length in mode 0
- Sensor in timing mode

The MEAS_RESET command ha to be sent before all other commands. In this state the measurement can be started by writing the MEAS_START address. By sending this signal the system will do a measurement, readout the sensor data and - if SENSOR_BLMEAS (counting mode) is set – also perform a measurement without trigger. This cycle is repeated as long as MEAS_COUNT is higher than cycle count (Figure 22).

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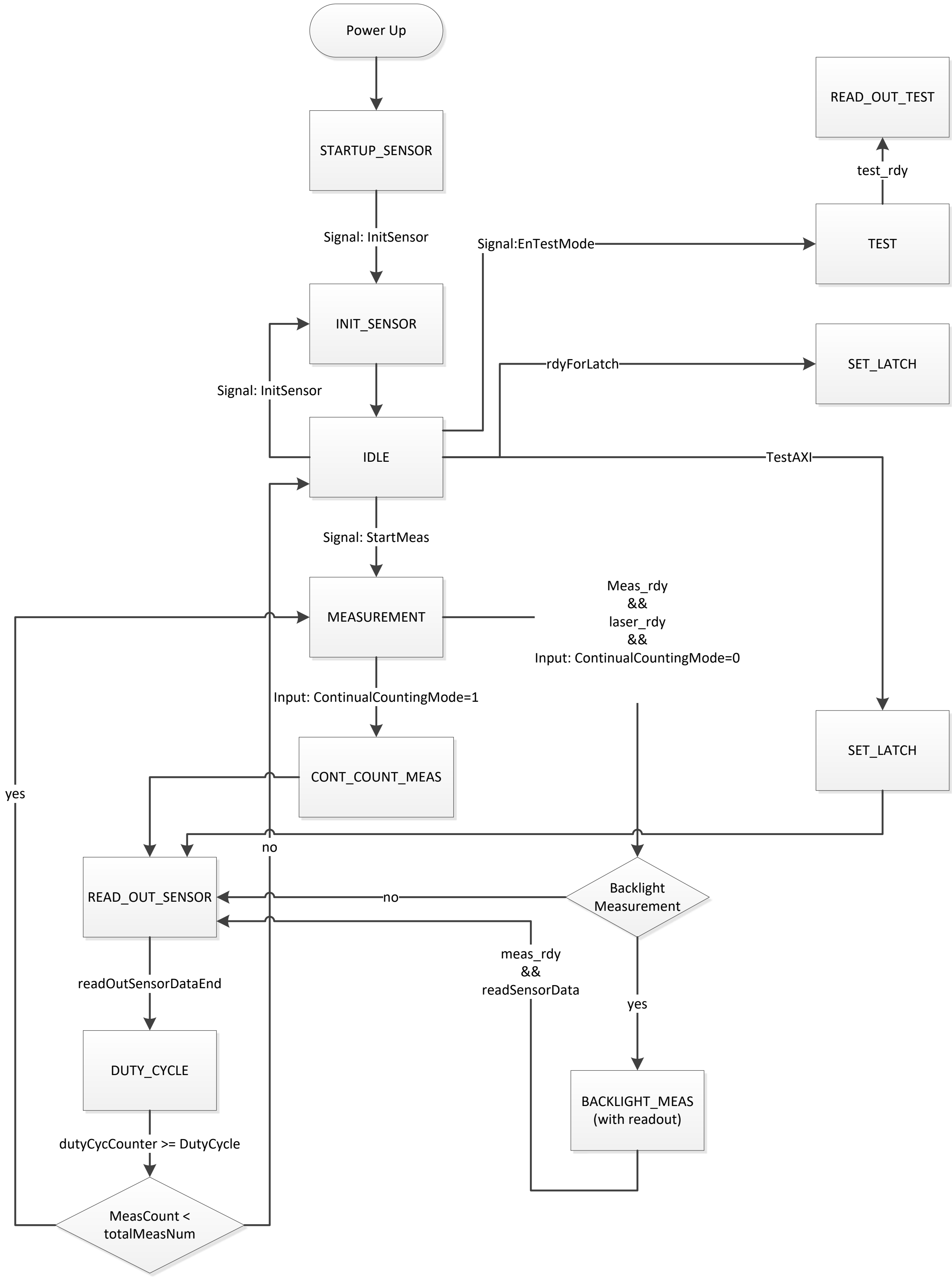

Figure 22: State diagram of firmware

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7.3 Configuration Registers

The configuration registers in the SoC provide the opportunity to change functions like timing, reference voltages and sensor mode different to initial state.
Table 3 to Table 10 show a list of addresses to access the registers. The tables contain base and offset addresses, respectively, name, description for the specific function with relevant bits in brackets and data length that have to be send behind the 8 bit address.

Base address	Name	Description
0x10	DAC	Digital to analog converter for reverence voltages
0x20	DELAY	Delay lines for trigger signals
0x30	MEAS	Measurement configurations
0x40	SENSOR	SPAD line sensor configurations
0x50	TRIGGER	Trigger configurations
0x70	TEST	Sensor test configurations

Table 3: Base addresses

Address offset	Name	Description	Data length
0x00	MEAS_COUNT	Number of measurements per Frame (16 bits)	2 bytes
0x01	MEAS_DUTY	Length of duty cycle, 1 bit correlates to 6,25 ns	2 bytes
0x02	MEAS_PREENSPAD	Time SPADs are activated before Gate, 1 bit correlates to 6,25 ns (10 bits)	2 bytes
0x03	MEAS_CT	Coincidence time*	96 bytes
0x04	MEAS_CD	Coincidence depth*	
0x05	MEAS_SN	SPAD enable*	
0x06	MEAS_CVSET	Set coincidence values and SPAD enable to sensor	0 byte
0x07	MEAS_GATEWIDTHCM	Gate width in counter/backlight mode, 1 bit correlates to 6,25 ns (13 bits)	2 bytes
0x08	MEAS_START	Starts on measurement for one frame	0 byte
0x09	MEAS_STOP	Stops measurements in infinity run mode	0 byte
0x0A	MEAS_RESET	Resets and initializes the sensor	0 byte
0x0B	MEAS_INFINRUN	Infinity measurements are done from start to manually set stop signal (1 bit)	1 byte
0x0C	MEAS_MTIMEGATECOUNT	Repetition number of clock shifts which is applied to Gate.	1 byte
0x0D	MEAS_TIMEGATECOUNT	Number of clock shifts which is applied to Gate.	1 byte
0x0E	MEAS_DELTATIMEGATE	Width of clock shifts on Gate in clocks. (6 bits)	1 byte
0x0F	MEAS_CONTCOUNTMODE	Invokes the Continual Counting Mode which is used for effective measurement and read-out. (1 bit)	1 byte

Table 4: MEAS offset addresses

*The first written data is applied to pixel 0 of row 0. For each pixel two bits are required, whereby the first written bit is MSB. The following Table 5 shows the binary values and the corresponding parameters.

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Value	Coincidence Time	Coincidence Depth	Active SPADs
00	1.5 ns	1 (disabled)	1
01	4.0 ns	2	2
10	8.0 ns	3	3
11	16.0 ns	4	4

Table 5: Description of CT, CD & SN values

Address offset	Name	Description	Data length
0x00	SENSOR_MODE	Sensor mode (1 bit) 0: timer mode 1: counting mode	1 byte
0x01	SENSOR_BLMEAS	Measurements without trigger (3 bits) 0: off 1 – 3: amount of BL measurements	1 byte
0x02	SENSOR_POWERSAVE	Sensor powersave mode (1 bit) 0: off 1: on	1 byte
0x03	SENSOR_REWRFREQ	Sensor Read/Write frequency (1 bit) 0: 20 MHz 1: 40 MHz	1 byte

Table 6: SENSOR offset addresses

Address offset	Name	Description	Data length
0x00	TRIGGER_MODE	Trigger mode (2 bits) 0: normal; both trigger at same time 1: speed; alternating triggers, double speed 2: separate; only one trigger depending on addr. TRIGGER_LR 3: off	1 byte
0x01	TRIGGER_LR	If in trigger mode 2 (1 bit) 0: left 1: right	1 byte
0x02	TRIGGER_PULSEWIDTH	Trigger pulse width 1 bit correlates to 6,25 ns (8 bits)	1 byte
0x03	TRIGGER_PRETRIG	Trigger time before gate 1 bit correlates to 6,25 ns (8 bits)	1 byte

Table 7: TRIGGER offset addresses

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Laser Components S.A.S.
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Fax: +33 1 39 59 53 50
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Address offset	Name	Description	Data length
0x00	DELAY_LEFT	1 bit correlates to 250 ps (8 bits)	1 byte
0x01	DELAY_RIGHT	1 bit correlates to 250 ps (8 bits)	1 byte

Table 8: DELAY offset addresses

Address offset	Name	Description	Data length
0x00	TEST_ENTESTMODE	sensor test mode (1 bit) 0: off 1: enable	1 byte
0x01	TEST_START	Starts one test cycle	1 byte
0x02	TEST_TDCSTART	Time of shifting TDCStart signal (8 bits) 1 bit correlates to 6,25 ns	1 byte

Table 9: TEST offset addresses

Address offset	Name	Description	Data length
0x00	DAC_VSELDT	DAC value(12 bits), 1 bit correlates to 805.9 µV	2 bytes
0x01	DAC_VENPLL		
0x02	DAC_VPLL2		
0x03	DAC_VPLL16		
0x04	DAC_VRESET		

Table 10: DAC offset addresses

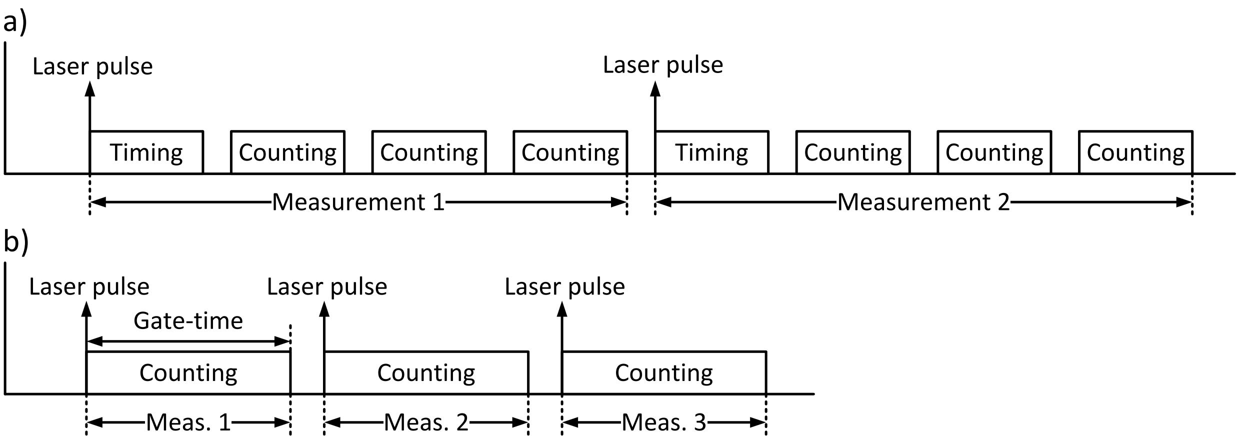

Figure 23: a) measuring procedure CONTCOUNTMODE=0
b) measuring procedure CONTCOUNTMODE=1

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Fax: +1 603 821-7041
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7.4 Timing description

Start a time measurement (Figure 24) by setting the Gate signal high. This enables the SPADs and the output of the front end circuitry. From this point on the TDC can be triggered by detected photons. The measurement ends after 1.28125 µs by setting the Gate signal low. By closing the Gate no further detection signal are transferred to the TDC preventing the measurement data from getting invalid.

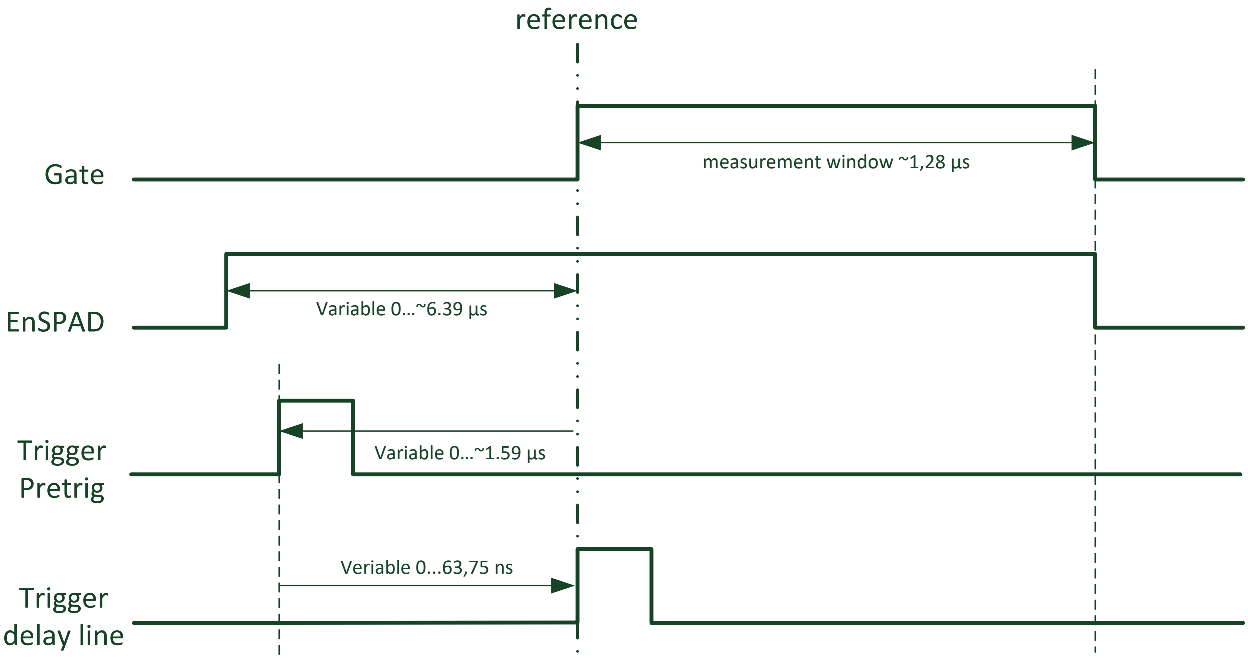

Figure 24: Timing of timing mode

To start a counting or BL measurement (Figure 25) Gate signal is to set high to enable the SPADs and the output of the front end circuitry. From this point on photon detection are counted by the integrated 8-bit-counter. Please note: no overflow protection is integrated. The counting ends with reaching the value MEAS_GATEWIDTHCM and setting Gate signal low. By closing the Gate no further detection signal are transferred to the counter.

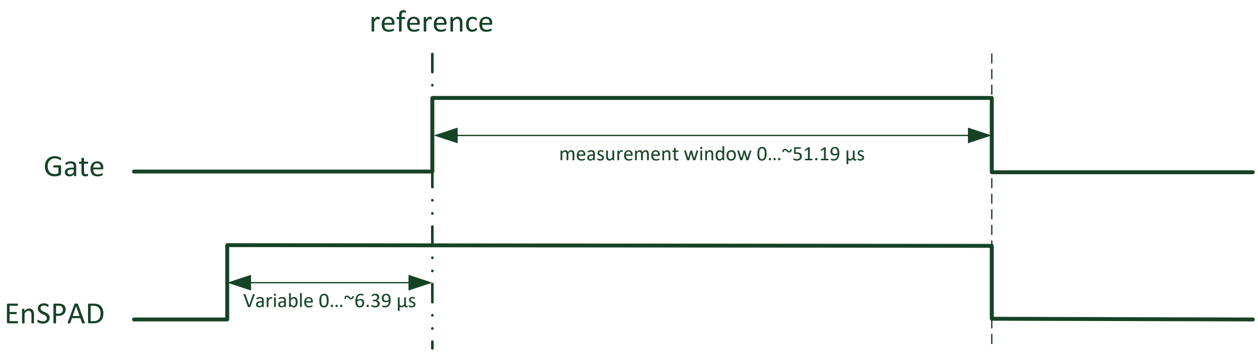

Figure 25: Timing of counting mode

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
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Optional in both measurement modes: EnSPAD signal can be set high prior to the Gate signal. Depending on MEAS_PREENSPAD it enables the SPADs and ensures that the reset phase of the SPADs, which takes about 10 ns time, is shifted out of the measurement window. With this the SPADs are ready for photon detection at the rinsing edge of the Gate signal.
Also optional in both measurement modes: The two trigger signals (left and right) can be set prior or post the gate signal. How long trigger signal is set high prior to the Gate signal depends on TRIGGER_PRETRIG value for both triggers. To set the Trigger signal high post Gate signal or for fine tuning, in combination with pre triggering, an individual delay for each of the two triggers can be set by DELAY_LEFT and DELAY_RIGHT values.

For TDC characterization a test mode (Figure 26) in pixel one is implemented. If test mode is enabled pixel one is connected permanently to the sensor output. In test mode the TDC is triggered by the external signal TDCStart instead of the SPADs. To start a test Gate signal is set high for 1.28125 µs. Within the measurement window TDCStart is set high depending on the TEST_TDCSTART value. With the rising edge of the event the TDC value is stored.

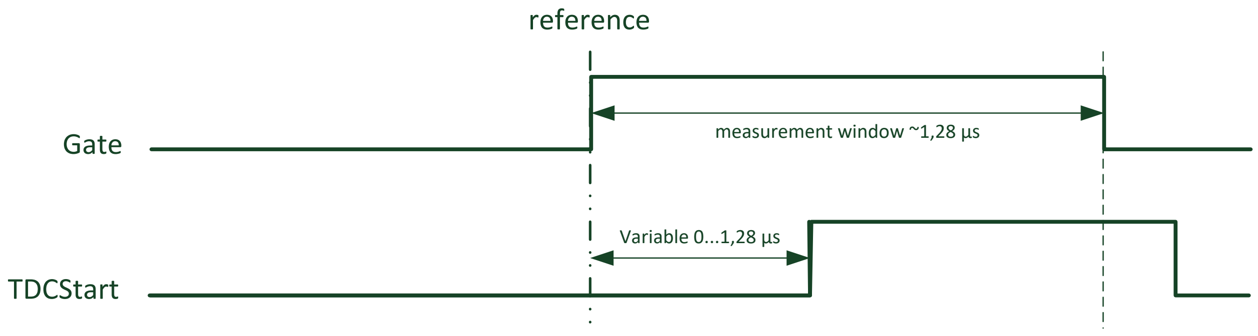

Figure 26: Timing of test mode

7.5 Time data

The two-stage TDC gives a 12-bit value representing the measured time. The final time value delivered from the sensor consists of three components which have to be combined off-chip.
Coarse is the time value measured by the coarse stage of the TDC. It is an 8-bit value representing the 8 MSB of the final 12-bit time value.

Start is a 4-bit value generated by the start-interpolator. It represents the time between the on-chip photon-generated start-signal (event) and the next rising edge of the coarse clock, at which the coarse TDC stage takes over the further measurement.

Stop is a 4-bit value generated by the stop-interpolator. It represents the time between the off-chip generated stop-signal and the next rinsing edge of the coarse clock, at which the coarse TDC stage stops the measurement.

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Laser Components S.A.S.
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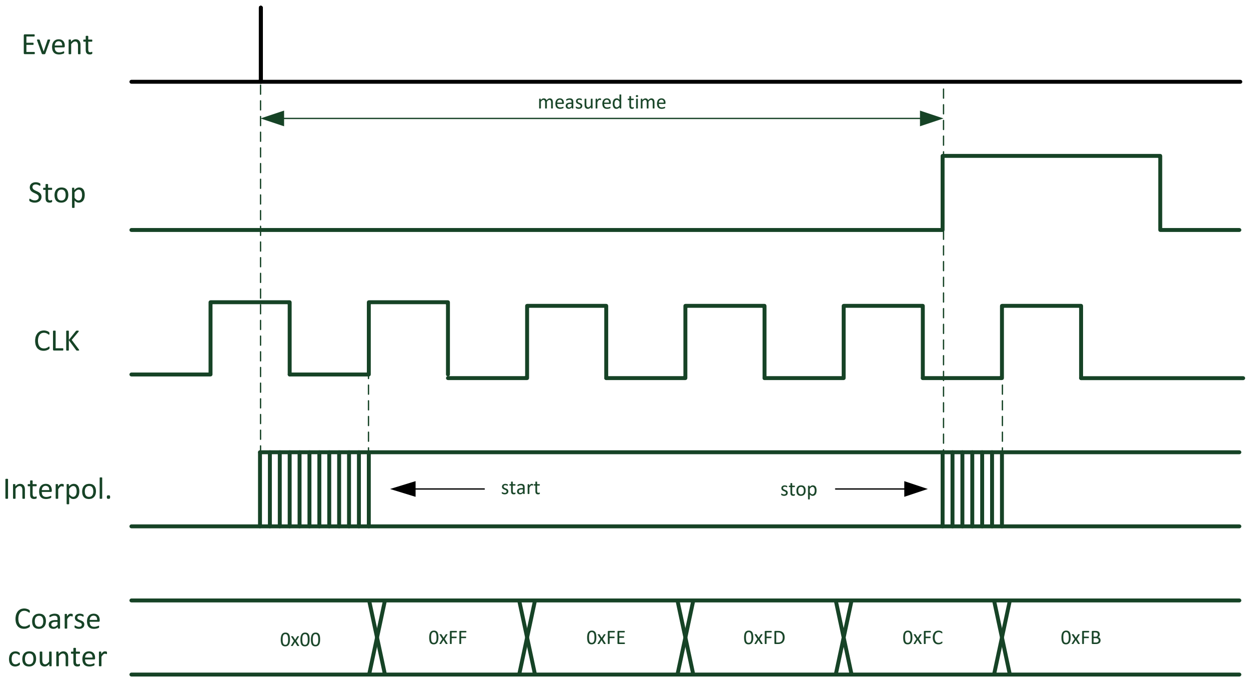

Figure 27: Timing diagram for time values description

To be noted: If N_{coarse} = 0x00 then no event is detected and equation below can be ignored. If $N_{coarse} \neq$ 0x00 all the outputs need to be inverted first before starting post processing.

- $\overline{N_{coarse}} = !(N_{coarse})$
- $\overline{N_{start}} = !(N_{start})$
- $\overline{N_{stop}} = !(N_{stop})$

The $\overline{N_{coarse}}$ is binary coded and can be used directly in the equation below. The $\overline{N_{start}}$ and $\overline{N_{stop}}$ are grey coded and need to perform grey code to binary conversion.

- $N_{binstart} = \text{greytobinary}(\overline{N_{start}})$
- $N_{binstop} = \text{greytobinary}(\overline{N_{stop}})$

The final time value is given by

$$T = \{4095 - (16(\overline{N_{coarse}}+1) + N_{binstart} - N_{binstop})\}T_{LSB}$$

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Laser Components S.A.S.
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Tel: +1 603 821–7040
Fax: +1 603 821–7041
info@laser-components.com
www.laser-components.com

8. Known bugs / Corrections

8.1 Change DAQ Value of DAC_VSELDT to 2000

For a better sensor performance in correlation to coincidence set the DAC_VSELDT (0x10) to decimal 2000 DN. It will adjust the deadtime of the SPADs.

Write command: 0x1007D0

8.2 Minimum of TRIGGER_PULSEWIDTH

The TRIGGER_PULSEWIDTH has to be >=2, otherwise with TRIGGER_PULSEWIDTH=1 the Trigger Channel is on high level all the time.

9. SPAD2L192

9.1 Summary

SPAD2L192 is a SPAD-based line sensor for direct time-of-flight application. The sensor composes 2 x 192 pixels with 4 SPADs each for adjustable photon coincidence detection. Time measurement is performed by a partially in-pixel time-to-digital converter with a resolution of 312.5 ps and a full range of 1.28 µs.

9.2 Features

- Supply 3.3 V for electronics and 31 V for SPADs
- Two line 192 pixel
- Variable coincidence time, coincidence depth, and number of active SPADs
- Timing and counting mode

Germany and Other Countries
Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

Nordic Countries
Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
Tel: +1 603 821–7040
Fax: +1 603 821–7041
info@laser-components.com
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9.3 Symbol and pinout

Figure 28: Floorplan SPAD2L192

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

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Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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info@laser-components.com
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Table 11 Interface

Signal	Pin #	Type	Default	Description
Reset	5	DI	0	Resetting of the sensor
Set	4	DI	0	Enables clock signal for coarse time measurement
Gate	8	DI	0	Enables output of the SPAD frontend circuit, defines measuring window, enables SPAD
Stop	11	DI	0	Stops time measurement
EnSPAD	50	DI	0	Enables SPAD (OR connected with Gate)
Clock	12	DI	-	100 MHz input clock for the DLL
EnDLL	48	DI	1	Enables control signal for in-pixel DLLs, turn off for power saving
ClkSel	62	DI	0	Enable DLLx2 bypass
EnRead	56	DI	0	Enables clock signal for data readout
ReWrClk	51	DI	-	20 MHz clock signal for data read and write
EnWrite	52	DI	0	Enables clock signal for data write
Mode	71	DI	0	Switch between timing (0) and counting (1) mode
DataCT0/1	2/81	DI	0	Input data for coincidence time (CT) for the lower (0) and upper (1) pixel line
DataCD0/1	3/82	DI	0	Input data for coincidence depth (CD) for the lower (0) and upper (1) pixel line
DataN0/1	83/80	DI	0	Input data for number of active SPADs for the lower (0) and upper (1) pixel line
Latch	49	DI	0	Applies input data to pixel circuit
TDCTest	77	DI	0	Enables TDC test mode
TDCStart	76	DI	0	Starts time measurement in TDC test mode

Signal	Pin #	Type	Default	Description
VcDLLx2Reset	1	AI	2.0 V	Reset voltage of DLLx2 (clock doubling)
Cathode	6/7	AI	31 V	Cathode voltage of the SPADs
VcDLLReset	19	AI	1.0 V	Reset voltage of the DLL
VpDLLx2	20	AI	1.3 V	External control voltage of DLLx2
SelDT	55	AI	2.0 V	Controls the SPAD dead time

08/21 / V05 / MaHF / manuals/diverse-spad/evaluation-board-spad21192

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Laser Components Germany GmbH
Tel: +49 8142 2864−0
Fax: +49 8142 2864−11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
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Signal	Pin #	Type	Description
Coarse	21, 16, 23, 24, 27…30	DO	Output of the counter
StartOut	33…36	DO	Output of the start interpolator
StopOut	39…42	DO	Output of the stop interpolator
Test0/1/2	15/18/22	DO	Test outputs: DLL phase 2/3 and sampling

Signal	Pin #	Type	Description
VcDLLOut	47	AO	Control voltage of the DLL
VcDLLx2Out	59	AO	Control voltage DLLx2 output for testing

9.4 Timing

9.4.1 Startup

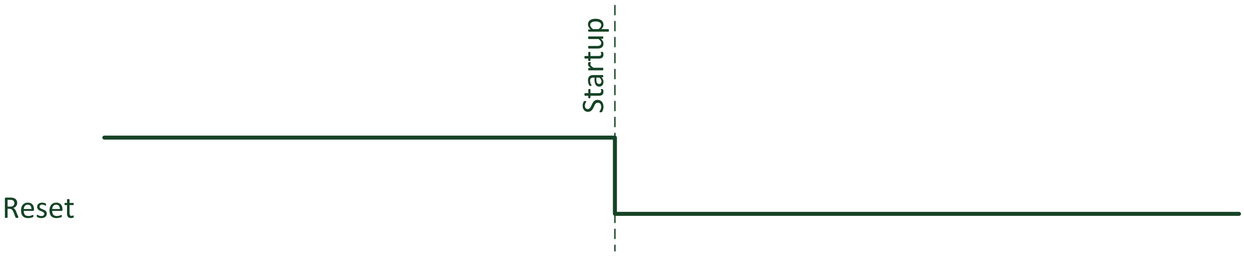

Figure 29: Timing sensor startup

After powering up the FPGA the **Reset** signal has to be set to high. Initiated by an external control signal **Reset** must switch to low signal. Now the sensor is ready for operation.

Germany and Other Countries
Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

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Laser Components USA, Inc.
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9.4.2 Timing Mode

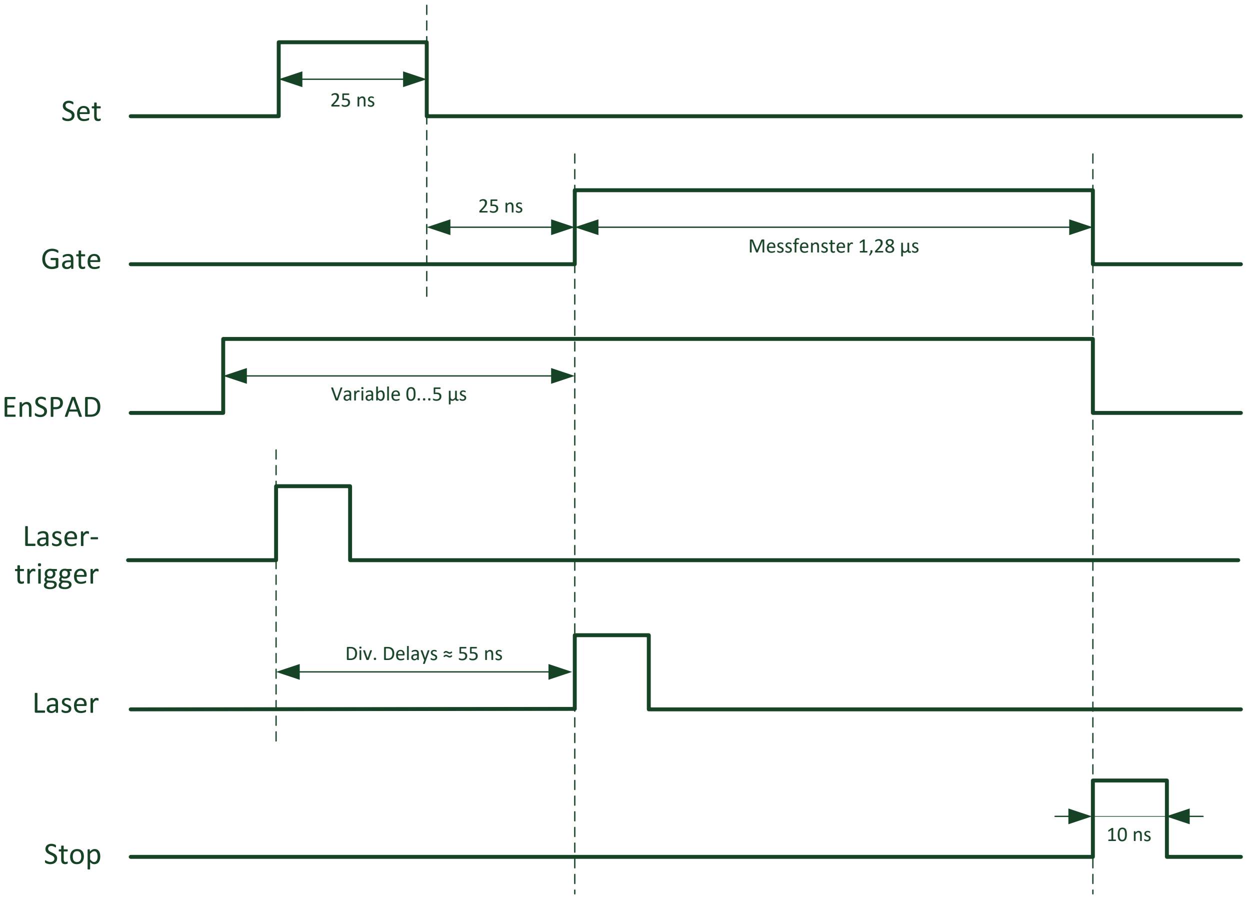

Figure 30: Timing sensor operation in timing mode

Before each time measurement a short 25 ns pulse at the **Set** signal is necessary to enable the 200 MHz clock for the coarse time measurement. After a short break of 25 ns the **Gate** signal is set to high to enable the output of the SPAD frontend circuit. Now SPAD generated pulses are able to start the time measurement. In standard scenario the laser pulse should be emitted with the beginning of the measurement window defined by **Gate**. To compensate for delays the laser has to be triggered some time before **Gate** is set high. To avoid the SPAD being reset during the measurement window, the SPADs can be enabled some time before the measurement window by setting **EnSPAD** to high. Since **EnSPAD** and **Gate** are connected via an OR gate for SPAD activation, EnSPAD has to remain in high state at least till **Gate** is set high. At the end of the measurement window the **Stop** signal has to be set high for at least 10 ns to stop the time measurement and transfer the time data into the in-pixel memory ready for readout.

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

Nordic Countries
Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
Tel: +1 603 821–7040
Fax: +1 603 821–7041
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9.4.3 Counting Mode

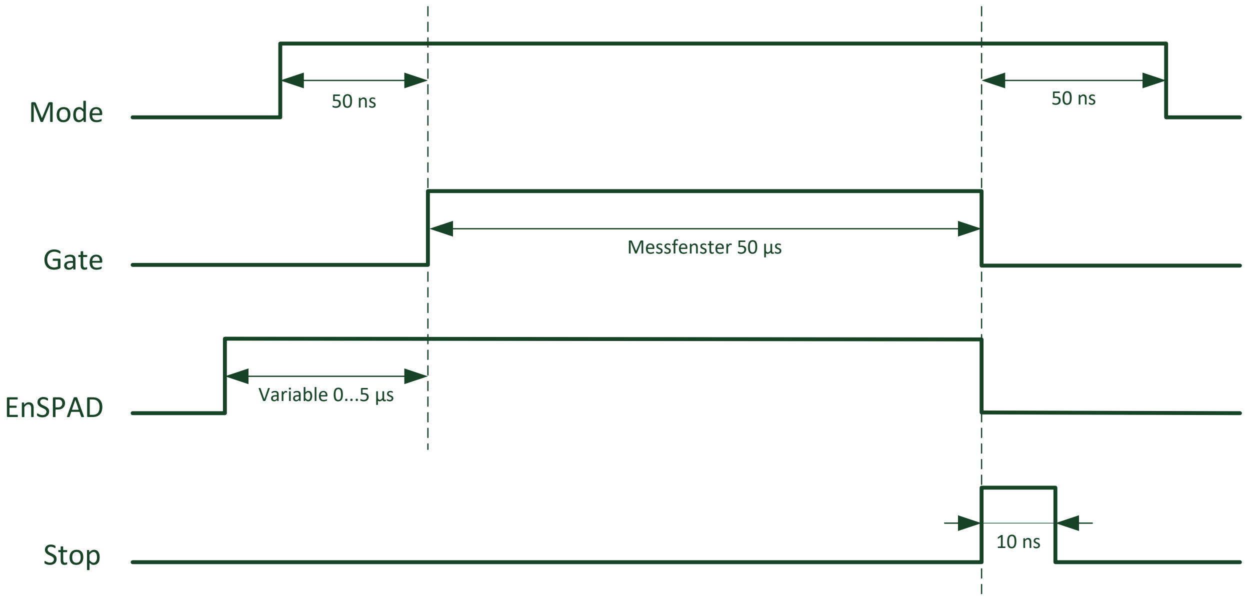

Figure 31: Timing sensor operation in counting mode

The count events the **Mode** has to be set to high. After a short break of 50 ns the **Gate** signal can be set high to enable the output of the SPAD frontend circuit. Now SPAD generated events are counted by the counter. After the measurement window **Stop** has to be set high for at least 10 ns to transfer the counter values to the in-pixel memory. As in timing mode the SPADs can also be enabled by setting **EnSPAD** high to avoid their reset within the measurement window.

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

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Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
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Fax: +1 603 821–7041
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9.4.4 Readout

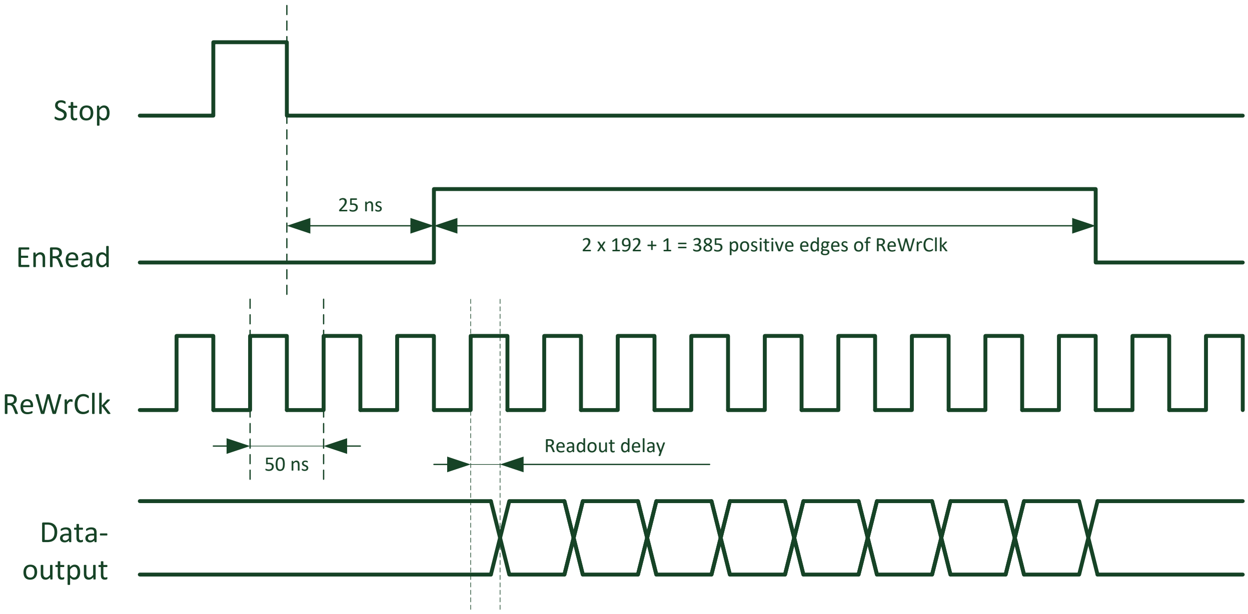

Figure 32: Timing sensor data readout

For data readout a short break of 25 ns between the **Stop** of the previous measurement has to be applied to transfer the data into the in-pixel memory. For readout the **EnRead** signal is set high at the falling edge of the **ReWrClk** and kept high for 385 clock periods. 384 clocks are for connecting the individual pixels to the readout bus while the last clock enables the internal pulldown buffers to avoid floating nets. Since the internal pixel change happens at the rising edge of the **ReWrClk**, the data should be captured at next rising edge to give enough time to process to the output pads.

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
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9.4.5 Write Data

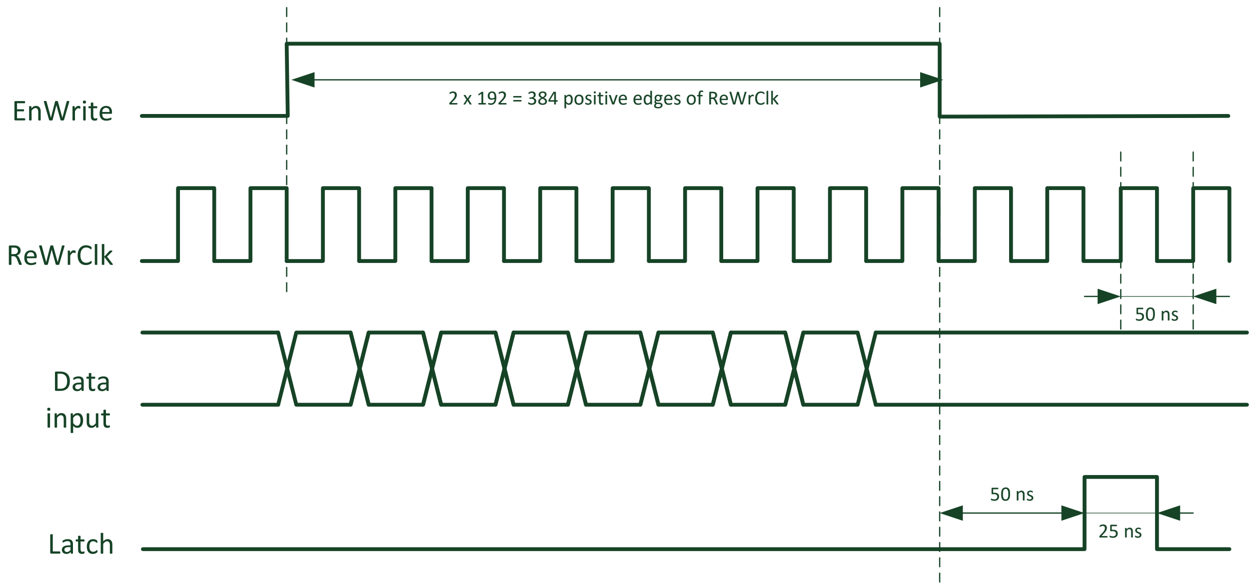

Figure 33: Timing sensor data writing

To write new data for the coincidence and enable SPAD registers, the **EnWrite** signal is set high at the falling edge of the **ReWrClk** and kept high for 384 clock periods. Since the data is internally captured at the rising edge of **ReWrClk**, the applied input data should be changed at the falling edge of the clock. After all data is written, at short pulse of 25 ns at **Latch** has to be applied to transfer the data from the shift register into the internal latches after a short break of 50 ns.

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Laser Components Germany GmbH
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Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

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Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

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Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
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Fax: +1 603 821–7041
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9.4.6 Test Mode

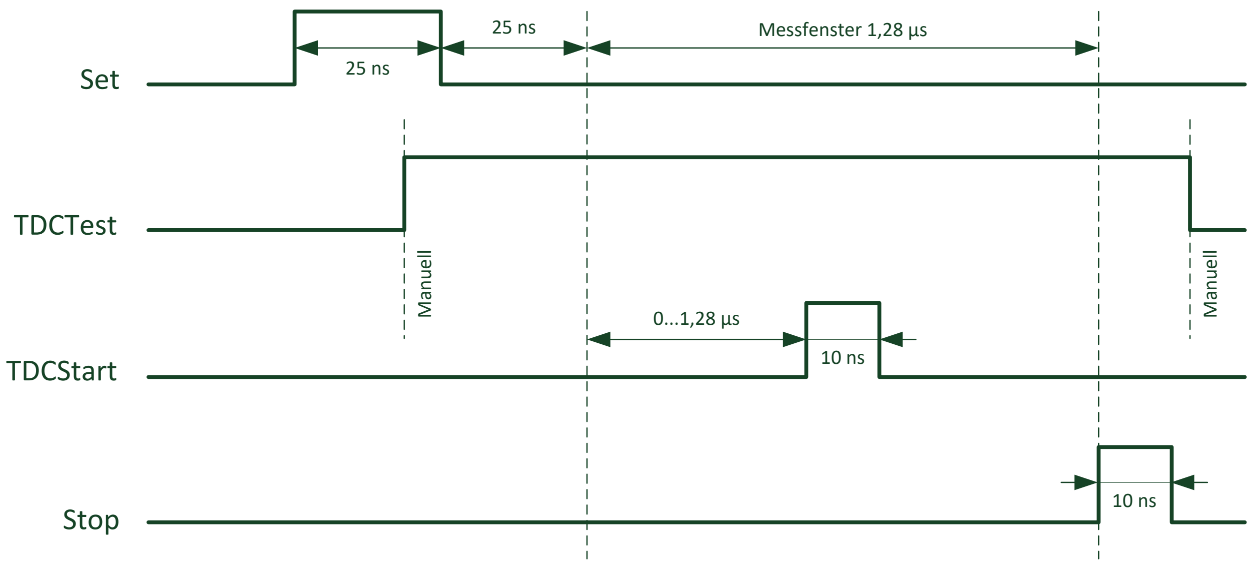

Figure 34: Timing sensor operation TDC test mode

In the TDC test mode the **TDCTest** has be set high. This can be done by the user. The enable the clock signal for coarse time measurement **Set** has to be set high for 25 ns before the measurements starts. The signal to start the time measurement **TDCStart** should be variable in time from 1,28 µs to 0 s before the **Stop** signal in steps of 312.5 ns or less. **TDCStart** and **Stop** signal must be high for at least 10 ns.

9.5 TDC Timing Calculation

The timing of the TDC is presented in Figure 35. The Start of the interpolator measures the time between start signal and the next positive edge of the clock. The next negative edge of the clock activates the counter and increments with the positives edges of the clock. The activation of the counter by the negative edge of the clock is taken by the synchronization circuit and therefore timing violations will be avoided. The same procedure will take place at the end of the measurement. The stop interpolator measures the time between the stop signal and the next positive edge of the clock. The stop of the counter will take place by the interruption of the clock at the next negative edge.

By means of the start interpolator N_{start}, the stop interpolator N_{stop} and the counter N_{coarse} the time T_{meas} can be calculated. It results in:

$$T_{meas} = \left(\frac{N_{start} - N_{stop}}{16} + N_{coarse} \right) T_{clk}$$

With the periodic duration of the clock T_{clk}. To enable a new measurement in the next cycle the clock will be activated before every measurement.

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Laser Components Germany GmbH
Tel: +49 8142 2864–0
Fax: +49 8142 2864–11
info@lasercomponents.com
www.lasercomponents.com

France
Laser Components S.A.S.
Tel: +33 1 39 59 52 25
Fax: +33 1 39 59 53 50
info@lasercomponents.fr
www.lasercomponents.fr

United Kingdom
Laser Components (UK) Ltd.
Tel: +44 1245 491 499
Fax: +44 1245 491 801
info@lasercomponents.co.uk
www.lasercomponents.co.uk

Nordic Countries
Laser Components Nordic AB
Tel: +46 31 703 71 73
Fax: +46 31 703 71 01
info@lasercomponents.se
www.lasercomponents.se

USA
Laser Components USA, Inc.
Tel: +1 603 821–7040
Fax: +1 603 821–7041
info@laser-components.com
www.laser-components.com

The Data of N_{start}, N_{stop} and N_{coarse} is stored inverted in the sensor. The start and the stop interpolator is grey code coded. Thus, the data of N_{start}, N_{stop} and N_{coarse} has to be inverted first. Second N_{start} and N_{stop} has to be converted from grey code to binary.

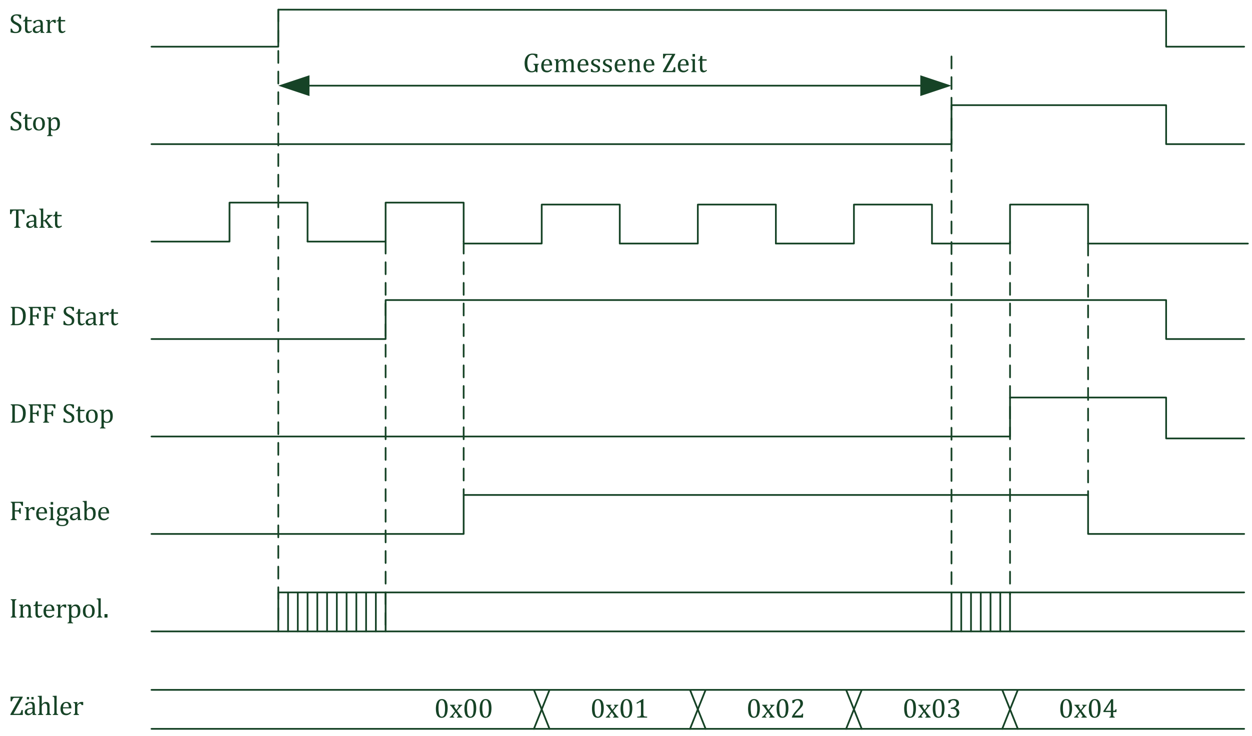

Figure 35: TDC timing diagram