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Industrial High Speed Optical Transceiver
IDL301T-220

APPLICATION NOTE

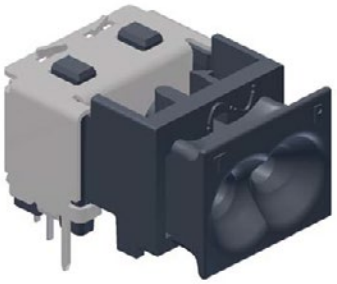
Firecomms

Firecomms IDL301T-220

High Immunity Fibre Optic Transceiver with Bare Fibre Connectivity

Design and Performance Guide

November 2010



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1. General Description of IDL301T-220 Transceiver

The IDL301T-220 is a 3.3V plastic optic fibre transceiver suitable for use in applications where very high electrical and electronic noise such as electromagnetic interference (EMI) is present. For example in AC motor drives for power generation the control circuits are routinely subjected to large EMI pulses. Furthermore, in certain medical devices and in RF applications such as inside a mobile phone tower antenna the control circuits are again exposed to large interference. Firecomms IDL301T transceiver is specifically designed to maintain data integrity right through the EMI burst.

Both internal tests and testing by customers and partners have verified the IDL301T as one of the most robust POF transceivers on the market today.

The transceivers incorporate a CMOS-based TX driver IC and a specially designed receiver ICs which provides extremely high immunity to general EMI/EMC, stray RF, and highly pulsed high voltage and current transitions as typically seen in application such as wind turbines and power systems equipment. The red 650nm light element is Firecomms' resonant cavity RCLED, a high speed LED that maintains level optical power over a very wide temperature range and hits a sweet spot for transmission in plastic optical fibre (POF).

This application note discusses good design practices that apply for the interface between the transceivers and, for example, an FPGA, ASIC, industrial Ethernet PHY or general controller. A description of the PCB layout is given for typical consumer housings used for these transceivers. Meeting electro-magnetic interference (EMI) and electro-static discharge (ESD) requirements and achieving maximum line performance depends on good design practices. These practices minimize high-speed digital switching noise and common-mode noise. They also provide shielding for the transceivers from each other and the general environment.

1.1. General Design Guidelines

Follow typical industry guidelines for designing and laying out the differential signals. Provide 100 Ohm termination on all high-speed switching signals. Provide impedance matching on long traces to prevent reflections.

1.2. General Controller - FOT Interface Application Circuit

The IDL301T-220 Transceivers have an input transmitter which accepts LVDS, LVPECL (3.3V) and CML driving signals. The DC off set voltage is 1.2V, which is directly compatible with LVDS. The input differential voltage swing across Data+ and Data- can range from 100mV to 1200mV, which is larger than the typical LVDS differential swing. The larger swing accommodates inputs from the full range of FPGA's, PHY's and ASIC's as well as general controllers. If the input is below 100mV the transmitter will switch down into a sleep mode where the light output is switched off and the unit consumes less than 40uA of current. It will wake up and start transmitting light as soon as the differential input exceeds 100mV. In general AC coupling to the data pins with 100uF high speed data capacitors is recommended.

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The receiver outputs an LVPECL differential voltage swing and must be terminated with the standard LVPECL resistor termination network as illustrated below. In general we recommend AC coupling of the data pins using 100uF high speed data capacitors.

The general recommendation for interfacing to any PHY IC is given in figure 1. It is recommended, in general, that AC coupling be used to avoid the problem of matching DC offsets between the FOTs and the PHY. If DC coupling is preferred, we recommend that you contact Firecomms sales for application support.

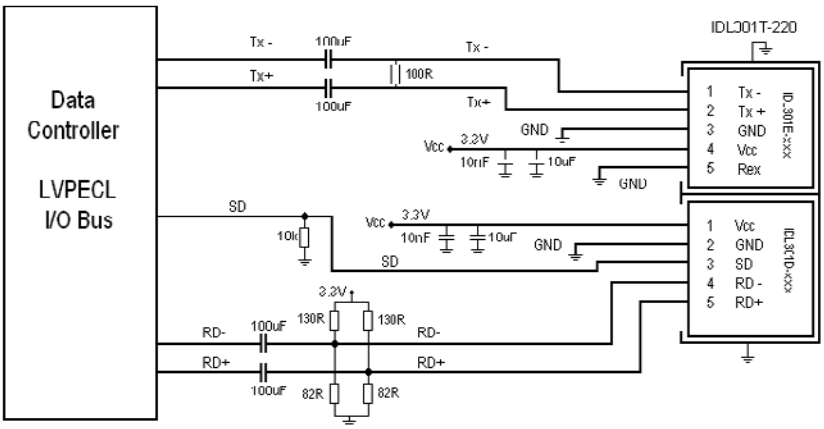

Figure 1: Schematic layout for an AC coupled IDL301T-220.

The circuit of figure 1 shows a 100 Ohm resistor on the FOT side of the Transmitter Data+ and Data- signal lines. This resistor is for 100 Ohm differential line impedance matching of the differential signal pair. This resistor should be located as close as possible to the AC coupling capacitors. The coupling capacitors should be located as close as possible to the PHY. Termination for the PHY should be arranged in accordance with the recommended individual PHY application circuit.

The receiver FOT requires a standard 130/82 Ohm PECL resistor termination network. In turn the AC coupling capacitors should be located as close to the PHY as possible and the termination on the PHY side of the coupling capacitors should be as recommended by the PHY manufacturer.

If the data controller is compatible with LVPECL and its application circuit recommends direct coupling to an LVPECL resistor termination network then it can be connected as illustrated in figure 2.

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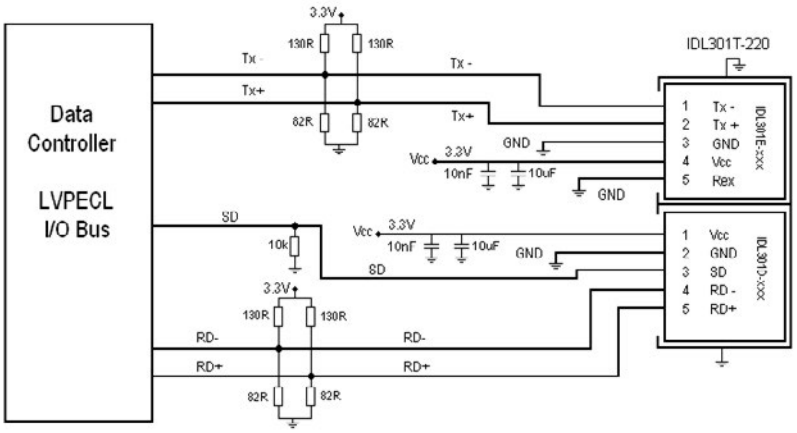

Figure 2: Schematic layout for a DC coupled IDL301T-220.

2. Optical and Electrical Cross Talk

Optical cross talk occurs when stray light from the transmitter FOT is picked up by the adjacent receiver FOT. The stray light from the transmitter interferes with the receiver and appears as signal noise. This reduces the overall system sensitivity. A physical barrier must be used to optically isolate the transmitter from the receiver. Electrical cross talk occurs when electro-magnetic pulses generated by the pulsing action of the transmitter induce current in the receiver and thereby add noise to the receiver and reduce overall system sensitivity. The metal barrier of the OptoLock housing provides an ideal isolation barrier between the TX and RX as well are protecting both devices from outside EMI/EMC.

3. Power and Ground Design and Filtering

Follow good design practices to minimize noise from digital switching and power supply circuits. Ensure the power supply is rated for the load. Keep power and ground noise levels below 50mV. Use bulk capacitors (4.7 – 10uF) between the power and ground planes to minimise power supply switching noise. Use 0.01uF decoupling capacitors to reduce high-frequency noise on the power and ground planes. For the 3.3V supply to the IDL301T-220 transceivers it is recommended to provide a separate supply line from the main 3.3V source to each of the transmitter and receiver FOT with a ferrite bead rated at 100mA and with a combined 10uF and 10nF filtering capacitor on each side of the ferrite bead to stop switching noise from travelling through the ferrite.

3.1. Power and Ground Planes

Provide ample power and ground planes. Avoid breaks in the ground plane especially in areas where it is shielding high-frequency signals. Route high-speed signals above a continuous ground plane. When possible fill unused areas of the signal planes with solid copper and attach them with via's to the ground plane that is not located adjacent to the signal layer. This technique, called "signal layer filling", can improve capacitive coupling of the power planes. When laying out ground planes care must be taken to

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avoid creating loop antenna effect. Run all ground planes as solid square or rectangular regions. Avoid creating loops with ground planes around other planes.

3.2. Differential Signal Layout

Route differential pairs close together and away from other signals. Keep both traces of each differential pair as identical to each other in length as possible. Use vias' to the ground plane (often referred to as tacking) on each side of the differential data line to ensure EMI and EMC are pulled to ground quickly. Keep each differential pair on the same plane. Minimize vias' and layer changes. Keep transmit and receive pairs away from each other. Run orthogonally, or separate with a ground plane layer.

4. *Mechanical Specifications*

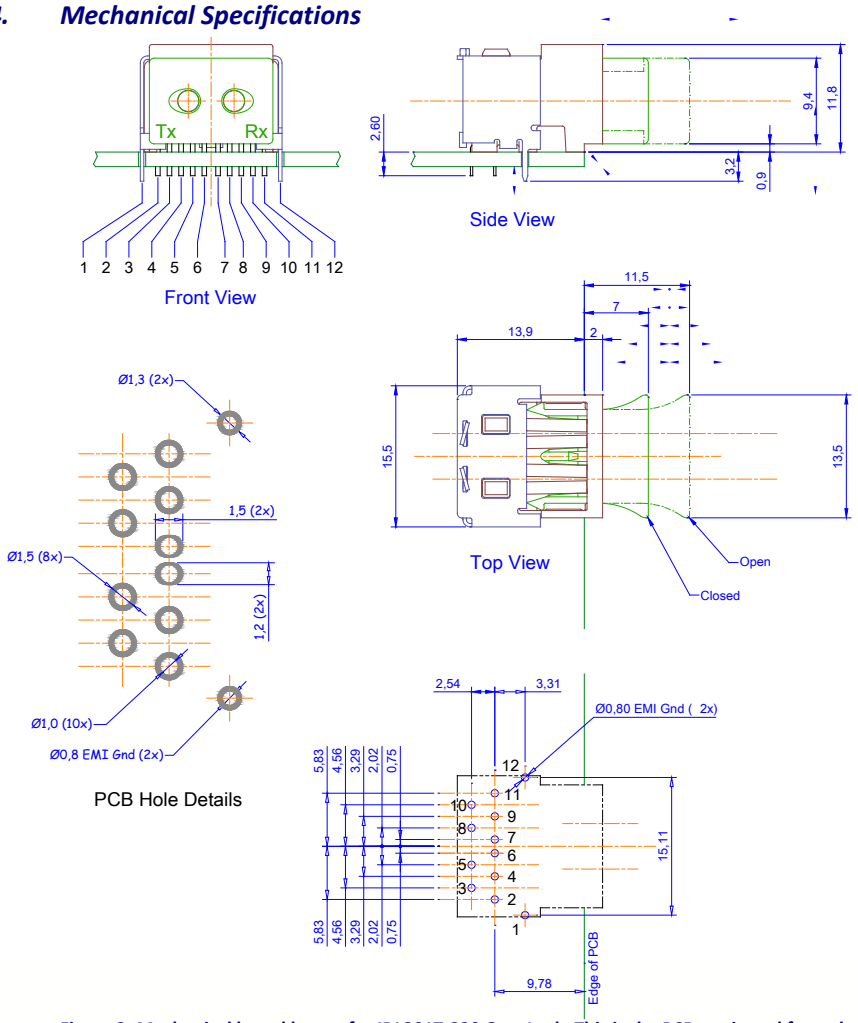

Figure 3: Mechanical board layout for IDL301T-220 OptoLock. This is the PCB as viewed from the top of the PCB looking down.

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5. Performance Results

The following results illustrate the performance of the IDL301T-220 across the allowed range for voltage supply (3.0V to 3.6V), the temperate range (-20°C to +85°C), the data speed rate and finally the optical power range.

5.1. Stability Over Voltage

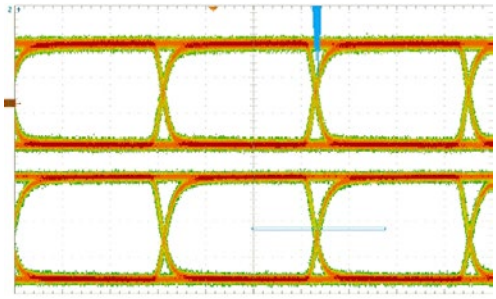

Figure 4: Receiver output at 3.0V, 125 Mbps, 25°C and mid-range optical power (-14dBm).

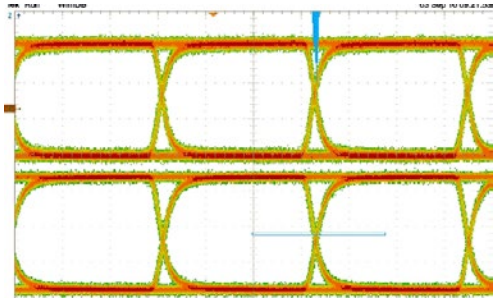

Figure 5: Receiver output at 3.3V, 125 Mbps, 25°C and mid-range optical power (-14dBm).

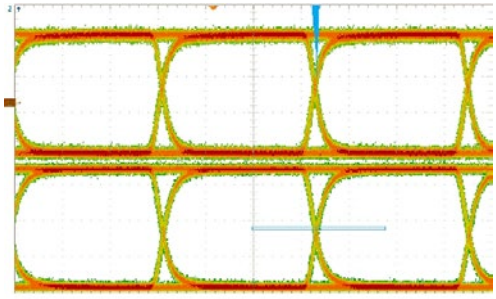

Figure 6: Receiver output at 3.6V, 125 Mbps, 25°C and mid-range optical power (-14dBm).

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5.2. Stability Over Temperature

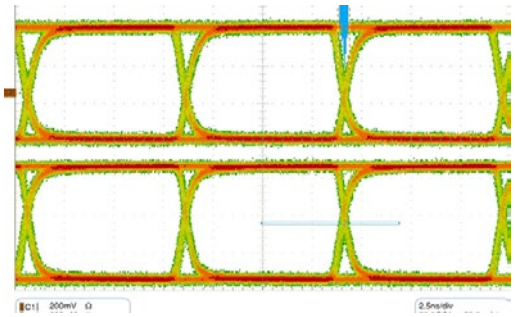

Figure 7: Receiver output at 3.3V, 125 Mbp, -20°C and mid-range optical power (-17dBm).

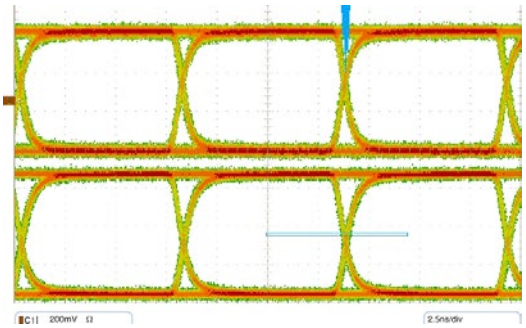

Figure 8: Receiver output at 3.3V, 125 Mbps, +25°C and mid-range optical power (-17dBm)

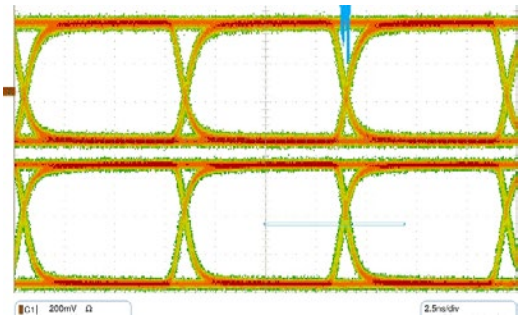

Figure 9: Receiver output at 3.3V, 125 Mbps, +85°C and mid-range optical power (-20dBm).

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5.3. Performance Across Optical power

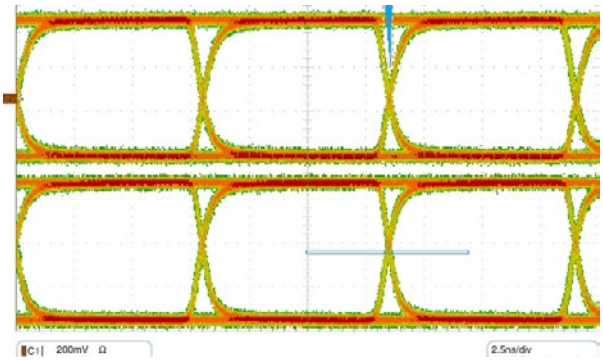

Figure 12: Receiver output at 3.3V, 125 Mbps, +25°C and mid-range optical power (-14dBm).

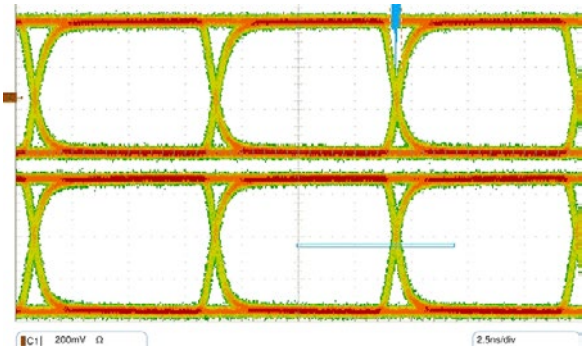

Figure 13: Receiver output at 3.3V, 125 Mbps, +25°C and mid-range optical power (-20dBm).

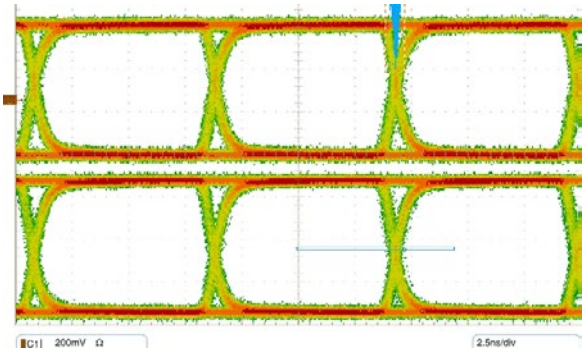

Figure 14: Receiver output at 3.3V, 125 Mbps, +25°C and mid-range optical power (-24dBm).

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6. EMI/EMC Immunity

6.1. Burst Tests

Burst tests were applied as follows. For each voltage amplitude level (positive and negative) from 500 to 4.5kV in 500V steps, 75 pulses at a frequency of 5kHz with a burst period of 300ms for a test duration of 120s were applied to a running data link with error counting. It was demonstrated that the data integrity was preserved right through the period of each burst with zero errors recorded up to ±4kV.

6.2. Direct ESD

ESD testing direct to the OptoLock was performed with increasing amplitude up to ±4kV. The results were full signal integrity was preserved (BER maintained during burst and non-burst data streaming).

6.3. Indirect ESD

Discharges were made to a plate located above the OptoLock simulating an ESD pulse impacting the machine casing. Positive and negative voltages were applied in increasing 500V steps. Full data integrity was preserved up to ±8kV discharges.

6.4. RF

EMI susceptibility was tested in a standard RF chamber. The test involved a frequency sweep from 30MHz to 1GHz in 2% intervals. No errors were recorded in data traffic during the sweep.

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