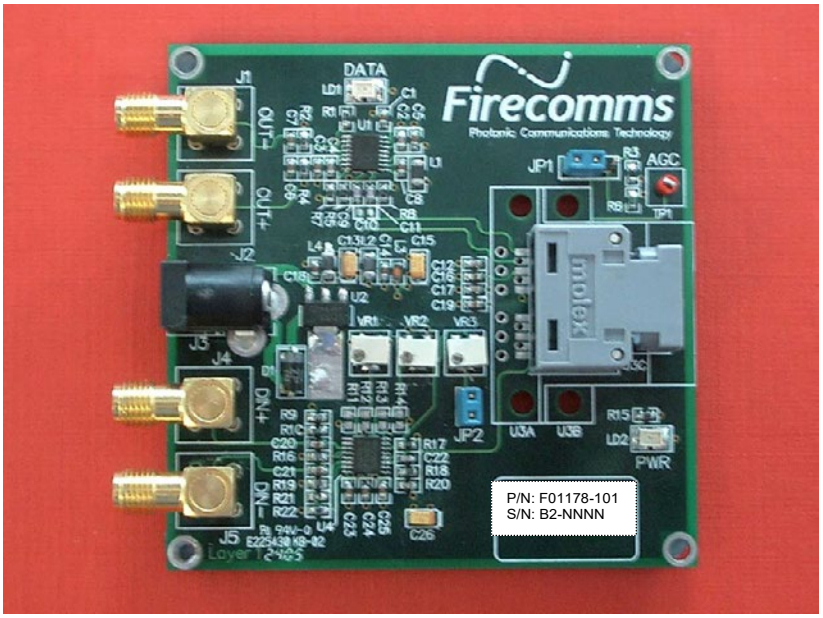
Application Note for F01178
FOT Tx:Rx Evaluation Board



Assembly: F01178-101 (FOT Tx:Rx with Molex SMI)
FOT Tx: FC300R
FOT Rx: FC300D

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Board Description

Firecomms F01178 evaluation board has been carefully laid out and tested to demonstrate the performance of the Firecomms FC300 Fibre Optic Transceivers (FOTs) over user defined lengths of Plastic Optic Fibre POF to the design maximum of 50m. The board takes differential Positive-ECL (PECL) data on the data input SMA connectors and drives the FOT transmit side. The board is designed so that the FOT's can be mounted in a through-hole SMI connector, or in a through-hole or surface mount style IDB 1394 connector. A POF link to a second board or in loop back mode (to link back to the Receive side of the FOT) is required. The receive side generates PECL level data signals available on +/- data-out SMA connectors.

The F01178-101 is fitted with a Molex SMI connector and Firecomms FC300R-120 Tx and FC300D-120 Rx FOT's. Contact Firecomms for information about other versions.

A Mindspeed MC2042-3 is used to drive the RCLED. The Receiver side of the FOT has an encapsulated PIN diode and TIA. A Mindspeed MC2044C is used as a Postamplifier / Quantizer. An on-board regulator accepts a dc input and provides power to the components on the board.

Refer to the FC300R/D Data sheets for detailed specifications of the Tx and Rx FOT's.

Specifications

Power -up

The board is powered by a standard 6 to 9V DC power jack (type D9, centre positive ⊕) which feeds a 3.3V DC power regulator to provide Vcc to the components on the board.

Input and output data require SMA connectors. The Input signals D_{in} and Inverse D_{in} are AC coupled. Biasing for the LED driver is performed on board after the AC coupling.

The PCB schematic is illustrated in Figure 1. The Physical size of the board and the silk screen layout are illustrated in Figure 2.

Figure 3a and 3b illustrates typical test setups with POF used in loop-back mode and in Network mode as separate Tx-Rx PCB's. Test data is given for these configurations for a 3m long loopback and also for 10m and 30m long POF links in Network mode, (see Figures 4, 5 and 6).

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Input Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	PECL input high (Data+ Data-)	-	-	800	mV
V_{IL}	PECL input low	200	-	-	mV
T_{ERJEF}	LVDS type output rise/fall times (1)	0.7	1	1.5	ns

Output Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{OH}	PECL output high (Data+ Data-)	-	-	800	mV
V_{OL}	PECL output low	200	-	-	mV
T_{ERJEF}	LVDS type output rise/fall times (1)	0.7	1	1.5	ns

Power Supply Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{supply}	PCB DC Supply	-	6	9	V
I_{supply}	Current drawn from DC supply	-	190	250	mA
V_{cc}	On board IC supply	2.97	3.3	3.63	V

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Circuit Schematic

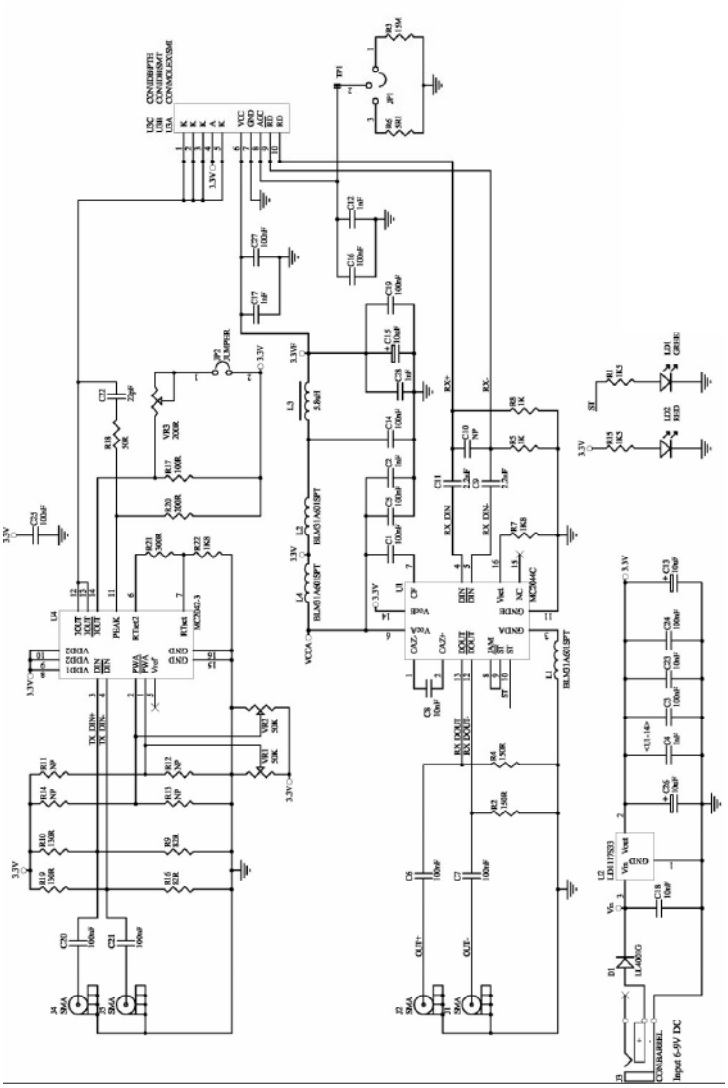

Figure 1: Schematic layout of the FOT Tx/Rx Evaluation Board.

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Physical Layout

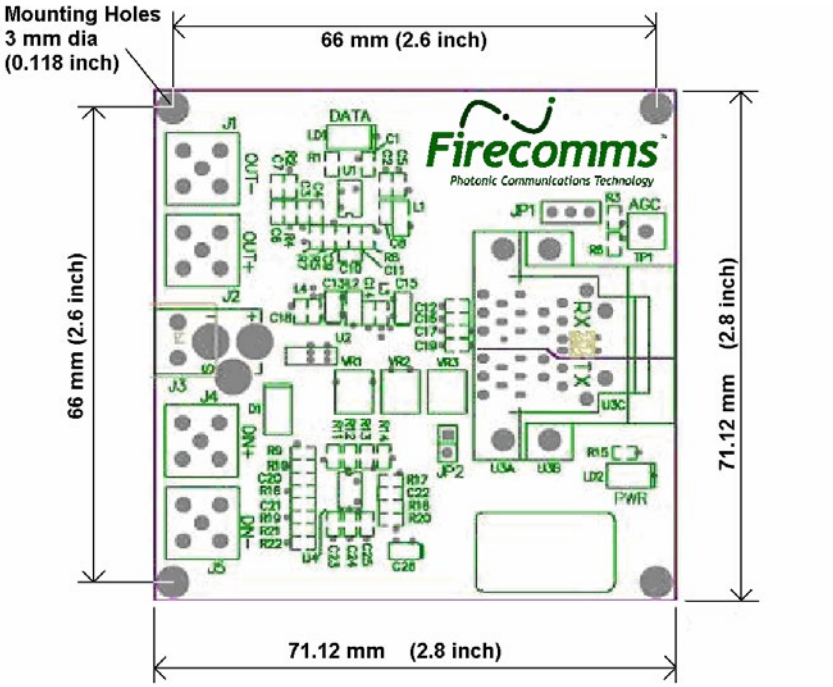

Figure 2: A Mechanical Drawing of the PCB for the F01178 Evaluation board.

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Typical Test Layouts

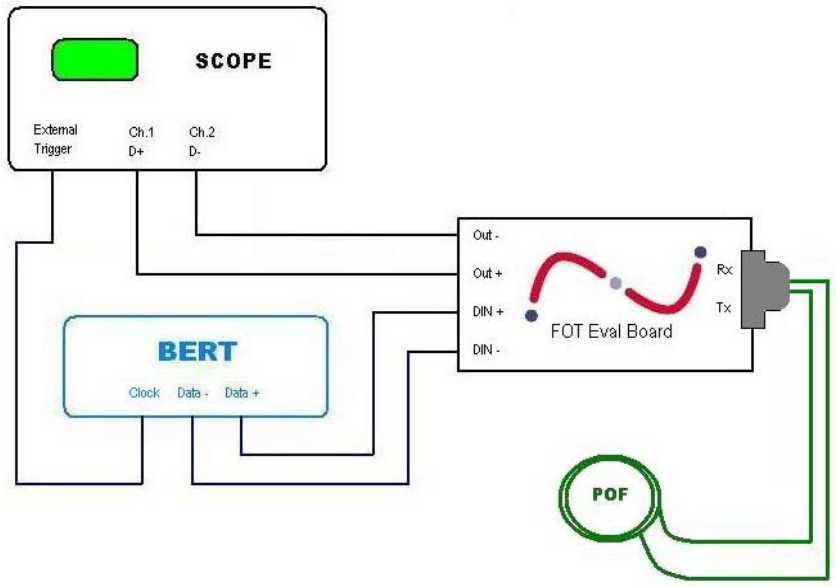

Figure 3a: Loop-back mode test setup.

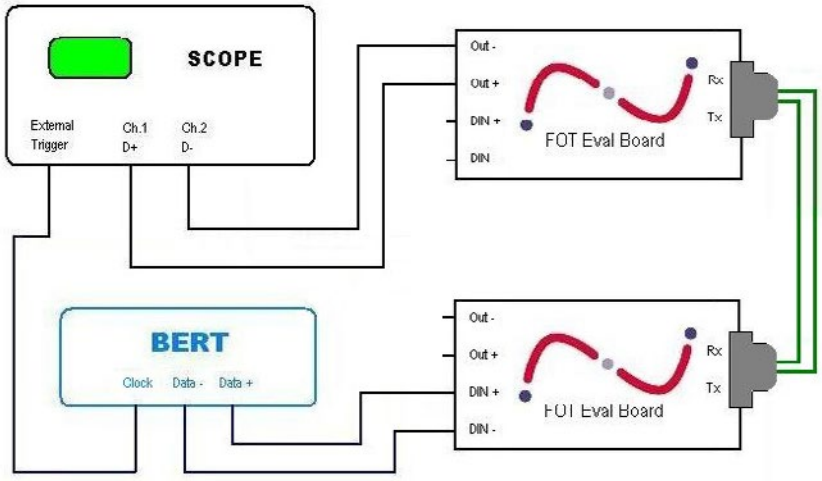

Figure 3b: Network mode test setup.

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Typical Test Data / Eye Diagrams

The following eye diagrams were taken using firstly a single evaluation board in Loopback mode over 3m of POF (as per Figure 3a) and secondly a pair of evaluation boards in Network mode (as per Figure 3b). Both experimental modes use a BERT running PRBS^7 at PECL level voltage (800mV pk-pk) to generate Data+ and Data- . The receive PECL signal is generated by connecting the Evaluation board output to a suitable oscilloscope. The oscilloscope is triggered by the BERT (see Figure 3a,3b). Figures 4, 5 and 6 below are the eye diagrams recorded. Figure 7 is a graph of the jitter results measured for a variety of POF lengths and over a temperature range from -10ºC to +70ºC.

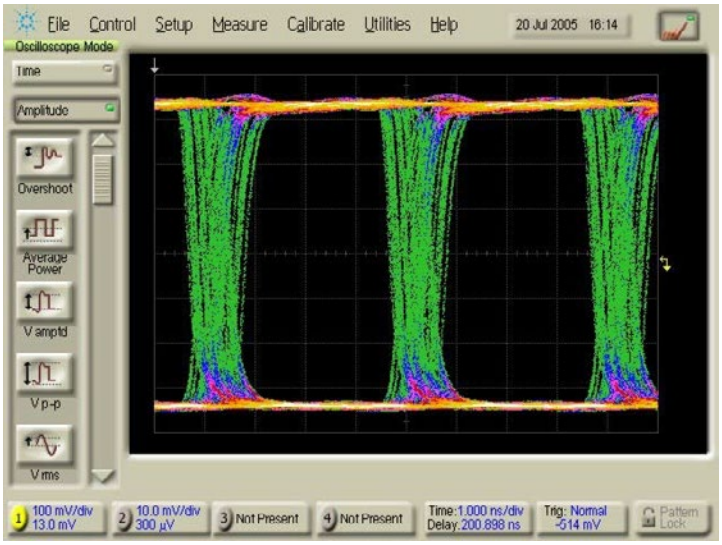

Figure 4: Evaluation board Eye Diagram in Loop-back mode over 3 m at 25ºC.

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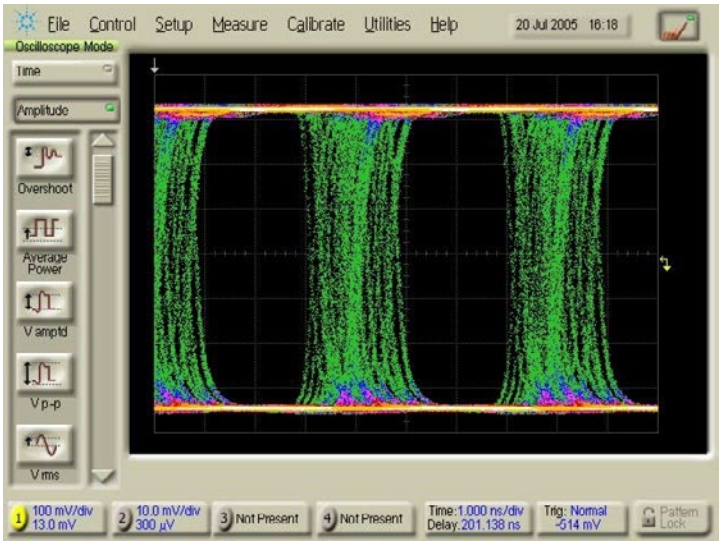

Figure 5: Evaluation board Eye Diagram in Network mode over 30m at 25ºC.

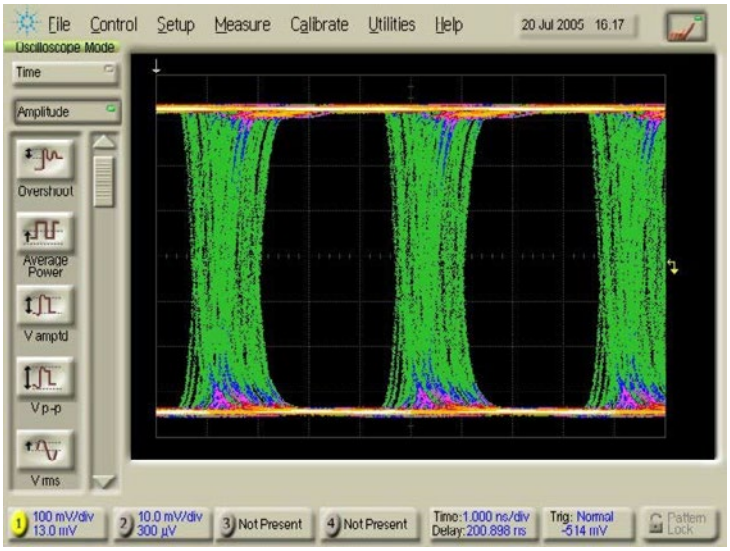

Figure 6: Evaluation board Eye Diagram in Network mode over 10m at 25ºC.

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Noise Performance

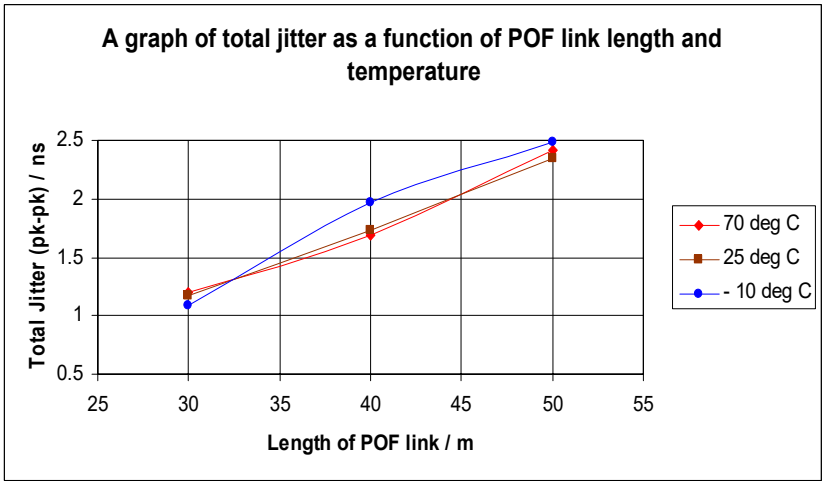

Figure 7: A graph of Jitter measured at TP4 from electrical eye diagrams taken from the Firecomms test board PECL signal.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. This could cause permanent damage to the pcb and or components. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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